TCAN1043xx-Q1 Low-Power Fault Protected CAN Transceiver with CAN FD and Wake

1 Features

- AEC Q100: Qualified for automotive applications
  - Temperature Grade 1: –55°C to 125°C, T_A
  - Device HBM classification level: ±16 kV
  - Device CDM classification level: ±1500 V
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Meets the requirements of the ISO 11898-2 (2016)
- All devices support classic CAN and 2Mbps CAN FD (flexible data rate) and "G" options support 5Mbps
  - Short and symmetrical propagation delays and fast loop times for enhanced timing margin
  - Higher data rates in loaded CAN networks
- V_{IO} Level shifting supports 2.8 V to 5.5 V
- Operating modes
  - Normal mode
  - Standby Mode with INH output and local and remote wake up request
  - Low power sleep mode with INH output and local and remote wake up request
- Passive behavior when unpowered
  - Bus and logic terminals are high impedance (no load to operating bus or application)
  - Hot plug capable: power up and down glitch free operation on bus and RXD output
- Meets or exceeds EMC standard requirements
  - IEC 62228-3 – 2007 compliant
  - SAE J2962-2 compliant
- Protection features
  - IEC ESD protection of bus terminals: ±8 kV
  - Bus fault protection: ±58 V (non-H variants) and ±70 V (H variants)
  - Undervoltage protection on supply terminals
  - Driver dominant time Out (TXD DTO): data rates down to 9.2 kbps
  - Thermal shutdown protection (TSD)
- Receiver common mode input voltage: ±30 V
- Typical loop delay: 110 ns
- Junction temperatures from –55°C to 150°C
- Available in SOIC (14) package and leadless VSON (14) package (4.5 mm x 3 mm) with improved automated optical inspection (AOI) capability

2 Applications

- 12-V or 24-V System applications
- Automotive and transportation
  - Advanced driver assistance system (ADAS)
  - Infotainment
  - Cluster
  - Body electronics and lighting

3 Description

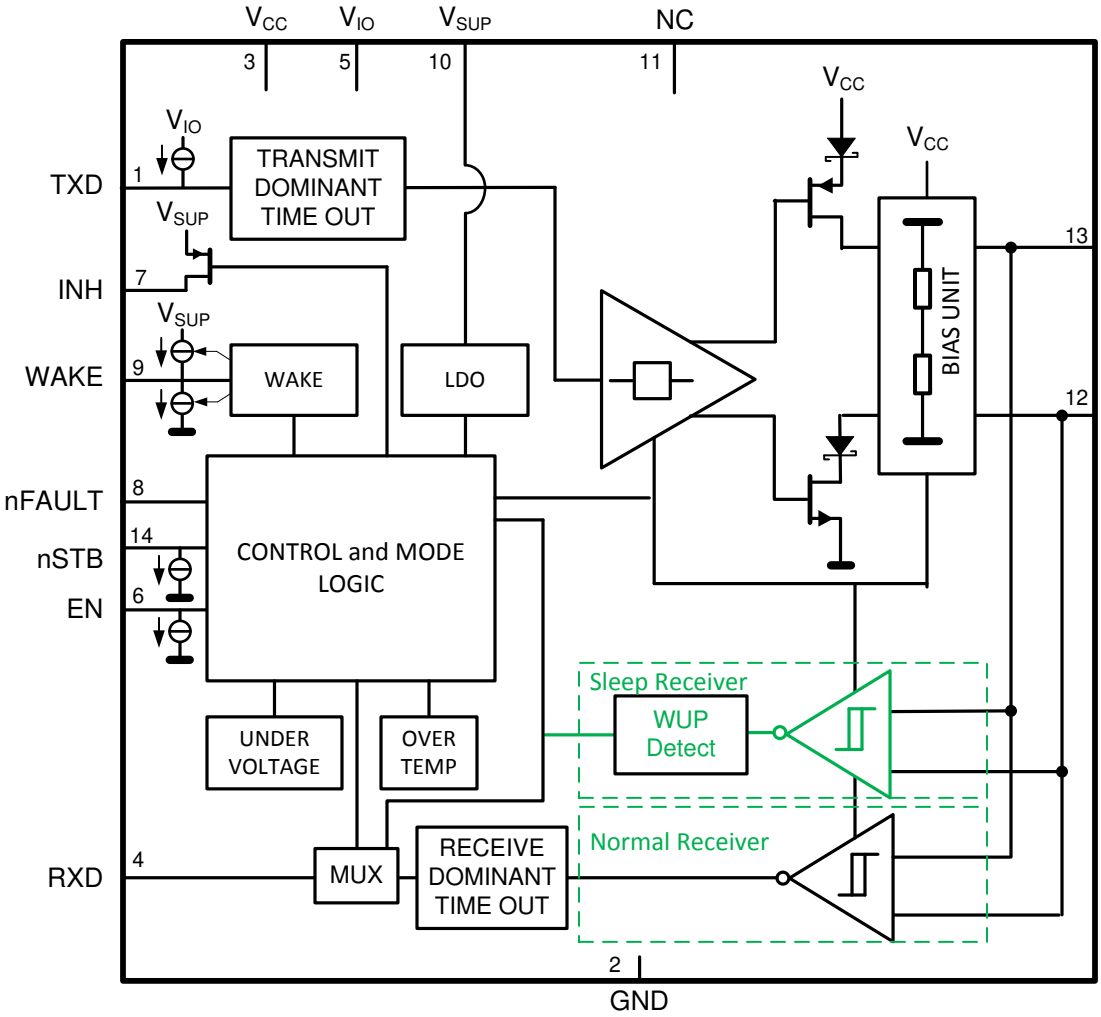
The TCAN1043xx-Q1 meets the physical layer requirements of the ISO 11898–2 (2016) High Speed Controller Area Network (CAN) specification providing an interface between the CAN bus and the CAN protocol controller. These devices support both classical CAN and CAN FD up to 2 megabits per second (Mbps). Devices with part numbers that include the suffix “G” are designed for CAN FD data rates up to 5Mbps. The TCAN1043xx-Q1 allows for system-level reductions in battery current consumption by selectively enabling (via the INH output pin) the various power supplies that can be present on a node. This allows an ultra-low-current sleep state in which power is gated to all system components except for the TCAN1043xx-Q1, which remains in a low-power state monitoring the CAN bus.

When a wake-up pattern is detected on the bus or when a local wake-up is requested via the WAKE input, the TCAN1043xx-Q1 initiates node start-up by driving INH high. The TCAN1043xx-Q1 includes internal logic level translation via the V_{IO} terminal to allow for interfacing directly to 3.3 V or 5 V controllers. The device includes many protection and diagnostic features including CAN bus line short-circuit detection and battery connection detection. The TCAN1043xx-Q1 meets the ESD and EMC requirements of IEC 62228-3 and J2962-2 without the need for additional protection components.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TCAN1043xx-Q1	SOIC (14)	8.65 mm × 6 mm
	VSON (14)	4.5 mm × 3 mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram

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4 Device Comparison Table

DEVICE NUMBER	BUS FAULT PROTECTION	MAXIMUM DATA RATE
TCAN1043-Q1	±58 V	2Mbps
TCAN1043H-Q1	±70 V	2Mbps
TCAN1043G-Q1	±58 V	5Mbps
TCAN1043HG-Q1	±70 V	5Mbps

5 Pin Configuration and Functions

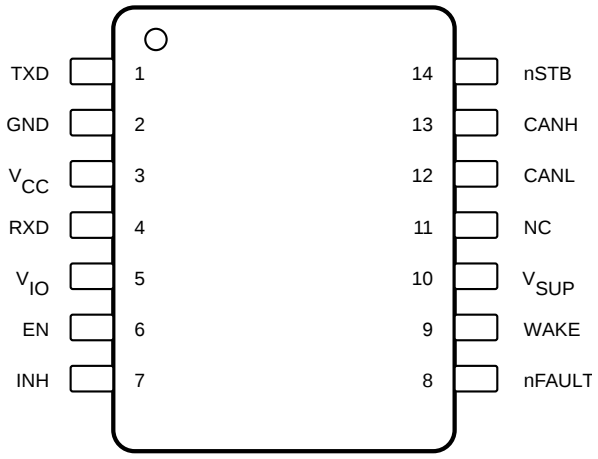


Figure 5-1. D Package, 14 Pin (SOIC) (Top View)

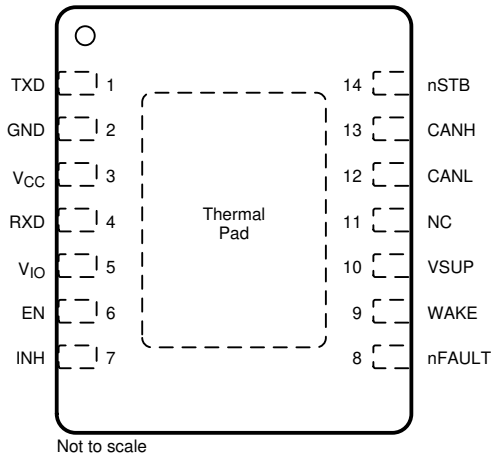


Figure 5-2. DMT Package, 14 Pin (VSON) Top View

Table 5-1. Pin Functions

PINS		TYPE	DESCRIPTION
NAME	NO		
TXD	1	Digital Input	CAN transmit data input (low for dominant and high for recessive bus states)
GND	2	GND	Ground connection
V_{CC}	3	Supply	5-V CAN bus supply voltage
RXD	4	Digital Output	CAN receive data output (low for dominant and high for recessive bus states), tri-state
V_{IO}	5	Supply	I/O supply voltage
EN	6	Digital Input	Enable input for mode control, integrated pull down
INH	7	High Voltage Output	Can be used to control system voltage regulators
nFAULT	8	Digital Output	Fault output, inverted logic
WAKE	9	High Voltage Input	Wake input terminal, high voltage input
V_{SUP}	10	Supply	Reverse-blocked battery supply input
NC	11	—	No connect (not internally connected)
CANL	12	Bus I/O	Low-level CAN bus input/output line
CANH	13	Bus I/O	High-level CAN bus input/output line
nSTB	14	Digital Input	Standby input for mode control, integrated pull down

6 Specifications

6.1 Absolute Maximum Ratings

See (1) (2)

			MIN	MAX	UNIT
V_{SUP}	Battery supply (reverse-blocked) voltage range – standard versions		–0.3	58	V
	Battery supply (reverse blocked) voltage range – H versions		–0.3	70	V
V_{CC}	5-V bus supply voltage		–0.3	7	V
V_{IO}	I/O level shifting voltage		–0.3	7	V
V_{BUS}	CAN bus I/O voltage range (CANH, CANL)	Devices without the "H" suffix	–58	58	V
	CAN bus I/O voltage range (CANH, CANL)	Devices with the "H" suffix	–70	70	V
$V_{(DIFF)}$	Max differential voltage between CANH and CANL	Devices without the "H" suffix	–58	58	V
		Devices with the "H" suffix	–70	70	V
$V_{(Logic\_Input)}$	Logic input terminal voltage range		–0.3	7	V
$V_{(Logic\_Output)}$	Logic output terminal voltage range		–0.3	7	V
V_{INH}	INH output pin voltage range	Devices without the "H" suffix	–0.3	58 and $V_O \le V_{SUP} + 0.3$	V
	INH output pin voltage range	H versions	–0.3	70 and $V_O \le V_{SUP} + 0.3$	V
$V_{(WAKE)}$	WAKE input pin voltage range	Devices without the "H" suffix	–0.3	58 and $V_I \le V_{SUP} + 0.3$	V
	WAKE input pin voltage range	H versions	–0.3	70 and $V_I \le V_{SUP} + 0.3$	V
$I_{O(LOGIC)}$	Logic output current	RXD, and nFAULT		8	mA
$I_{O(INH)}$	INH output current			4	mA
$I_{O(WAKE)}$	Wake current if due to ground shifts $V_{(WAKE)} \le V_{(GND)} – 0.3$ V, thus the current into WAKE must be limited via an external serial resistor			3	mA
T_J	Operating virtual junction temperature range		–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002	V_{SUP}, INH(1)	±4000	V
			All pins, except V_{SUP}, INH(1)	±6000	V
			CAN bus terminals (CANH, CANL)(2)	±16000	V
		Charged device model (CDM) - SOIC	All terminals(3)	±1500	V
		Charged device model (CDM) - DMT	All terminals(3)	±500	V
			Corner terminals(3)	±750	V
		Machine model (MM)	All terminals(4)	±200	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Test method based upon AEC-Q100-002, CAN bus terminals stressed with respect to each other and to GND.
(3) Tested in accordance to AEC-Q100-011.
(4) Tested in accordance to JEDEC Standard 22, Test Method A115A.

6.3 ESD Ratings IEC Specification

				VALUE	UNIT
$V_{(ESD)}$	System level electrostatic discharge (ESD)	CAN bus terminals (CANH, CANL) to GND	ISO 10605 per SAE J2962-2: Powered Air Discharge(2)	±15000	V
			ISO 10605 per SAE J2962-2: Powered Contact Discharge(2)	±8000	V
			IEC 61000-4-2 (150 pF, 330 Ω): Unpowered contact discharge	±15000	V
		V_{SUP} and WAKE	IEC 61000-4-2 (150 pF, 330 Ω) Unpowered contact discharge	±6000	V
	ISO 7637-2 Transients according to GIFT - ICT CAN EMC test specification(1)	CAN bus terminals (CANH, CANL) to GND, V_{SUP}, WAKE	Pulse 1	–100	V
			Pulse 2	+75	V
			Pulse 3a	–150	V
			Pulse 3b	+100	V
	ISO 7637-3 Transients	CAN bus terminals (CANH, CANL) to GND, V_{SUP}, WAKE	Direct coupling capacitor "slow transient pulse" with 100-nF coupling capacitor - powered	±85	V

(1) ISO 7637 is a system level transient test. Results given here are specific to the IBEE CAN EMC Test specification conditions. Different system level configurations leads to different results.
(2) Verified by external test facility on SOIC package

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{SUP}	Battery supply (reverse-blocked) voltage range - standard version	4.5		45	V
	Battery supply (reverse-blocked) voltage range - H version	4.5		60	V
V_{CC}	5 V Supply Voltage	4.5		5.5	V
V_{IO}	I/O supply voltage	2.8		5.5	V
$I_{OH(LOGIC)}$	Logic terminal high level output current – RXD and nFAULT	–2			mA
$I_{OL(LOGIC)}$	Logic terminal low level output current – RXD and nFAULT			2	mA
$I_{O(INH)}$	INH output current			1	mA
T_A	Operational free-air temperature	–55		125	°C

6.5 Thermal Information

THERMAL METRIC(1)		TCAN1043x-Q1		UNIT
		D (SOIC)	DMT (VSON)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78	33.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.6	30.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.7	10.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.7	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	34.3	10.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Dissipation Ratings

PARAMETER		TEST CONDITIONS	POWER DISSIPATION	UNIT
P_D	Average power dissipation	V_{SUP} = 14 V, V_{CC} = 5 V, V_{IO} = 5 V, T_J = 27°C, R_L = 60 Ω, nSTB = 5 V, EN = 5 V, C_{L_RXD} = 15 pF. Typical CAN operating conditions at 500 kbps with 25% transmission (dominant) rate.	58	mW
		V_{SUP} = 14 V, V_{CC} = 5.5 V, V_{IO} = 5.5 V, T_J = 150°C, R_L = 50 Ω, nSTB = 5.5 V, EN = 5.5 V, C_{L_RXD} = 15 pF. Typical high load CAN operating conditions at 1Mbps with 50% transmission (dominant) rate and loaded network.	126	mW
T_{TSD}	Thermal shutdown temperature		170	°C
T_{TSD_HYS}	Thermal shutdown hysteresis		10	°C

6.7 Electrical Characteristics

Over recommended operating conditions with T_A = –55°C to 125°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
SUPPLY CHARACTERISTICS							
I_{SUP}	Supply current V_{SUP}	Normal, Silent, Go-to-Sleep			40	70	µA
		Standby mode	Standby mode, V_{CC} > 4.5 V, V_{IO} > 2.8 V, V_{INH} = $V_{(WAKE)}$ = V_{SUP}		15	45	µA
		Sleep mode	Sleep mode, V_{CC} = V_{IO} = V_{INH} = 0 V $V_{(WAKE)}$ = V_{SUP}		15	30	µA
I_{CC}	Supply current Normal mode V_{CC}	Dominant	See Figure 7-2. TXD = 0 V, R_L = 60 Ω, C_L = open. Typical bus load.			70	mA
			See Figure 7-2. TXD = 0 V, R_L = 50 Ω, C_L = open. High bus load.			80	mA
		Dominant with bus fault	See Figure 7-2. TXD = 0 V, CANH = -25 V, R_L = open, C_L = open			110	mA
		Recessive	See Figure 7-2. TXD = V_{IO}, R_L = 50 Ω, C_L = open, R_{CM} = open			5	mA
	Supply current Silent and Go-to-Sleep mode		See Figure 7-2. TXD = V_{IO}, R_L = 50 Ω, C_L = open			2.5	mA
	Supply current Standby mode		See Figure 7-2. EN = L, NSTB = L			5	µA
	Sleep mode		See Figure 7-2. EN = H or L, NSTB = L			5	
I_{IO}	I/O supply current	Normal mode	RXD floating, TXD = 0 V (dominant) nSTB = V_{IO}, EN = V_{IO}			450	µA
		Normal, Silent or Go-to-Sleep mode	RXD floating, TXD = V_{IO} recessive			5	µA µA
		Sleep mode	NSTB = L			5	µA
UV_{SUP}	Undervoltage detection on V_{SUP} for protected mode			3.0		4.2	V
$V_{HYS(UVSUP)}$	Hysteresis voltage on UV_{SUP}				50		mV
UV_{VCC}	Rising undervoltage detection on V_{CC} for protected mode				4.1	4.4	V
	Falling undervoltage detection on V_{CC} for protected mode			3.5	3.9		V
$V_{HYS(UVVCC)}$	Hysteresis voltage on UV_{VCC}				200		mV
UV_{VIO}	Undervoltage detection on V_{IO} for protected mode			1.3		2.75	V
$V_{HYS(UVIO)}$	Hysteresis voltage on UV_{IO}				80		mV
Driver Electrical Characteristics							
$V_{O(D)}$	Bus output voltage dominant - normal mode	CANH	See Figure 7-2 and Figure 8-3, TXD = 0 V, Normal mode, 50 ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{O(R)}$	Bus output voltage recessive	CANH and CANL	See Figure 7-2 and Figure 8-3, TXD = V_{CC}, V_{IO} = V_{CC}, Normal or Silent[2], R_L = open, R_{CM} = open	2	0.5 × V_{CC}	3	V

6.7 Electrical Characteristics (continued)

Over recommended operating conditions with T_A = –55°C to 125°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
$V_{OD(D)}$	Differential output voltage dominant	CANH - CANL	See Figure 7-2 and Figure 8-3, TXD = 0 V, Normal mode, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	1.5		3	V
			See Figure 7-2 and Figure 8-3, TXD = 0 V, Normal mode, 45 Ω ≤ R_L ≤ 50 Ω, CL = open, R_{CM} = open	1.4		3	V
			See Figure 7-2 and Figure 8-3, TXD = 0 V, Normal mode, R_L = 2240 Ω, C_L = open, R_{CM} = open	1.5		5	V
			See Figure 7-2 and Figure 8-3, TXD = 0 V, Normal mode, 45 Ω ≤ R_L ≤ 70 Ω, C_L = open, R_{CM} = open	1.4		3.3	V
$V_{OD(R)}$	Differential output voltage recessive	CANH - CANL	See Figure 7-2 and Figure 8-3, TXD = V_{CC}, Normal or Silent mode[2], R_L = 60 Ω, C_L = open, R_{CM} = open	–120		12	mV
			See Figure 7-2 and Figure 8-3, TXD = V_{CC}, Normal or Silent mode[2], R_L = open, C_L = open, R_{CM} = open	–50		50	mV
V_{SYM}	Driver symmetry, dominant or recessive V_{SYM} = ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}		See Figure 7-2 and Figure 9-4, Normal mode, C_L = open, R_{CM} = open, TXD = 1MHz[3]	0.9		1.1	V / V
V_{SYM_DC}	Driver symmetry, dominant $V_{SYM(DC)}$ = V_{CC} - $V_{O(CANH)}$ - $V_{O(CANL)}$		See Figure 7-2 and Figure 8-3, Normal or Silent mode, R_L = 60 Ω, C_L = open, R_{CM} = open	–400		400	mV
$I_{OS(DOM)}$	Short circuit steady-state output current dominant		See Figure 7-10 and Figure 8-3, V_{CANH} = -5 V, CANL = open, TXD = 0 V	–100			mA
			See Figure 7-10 and Figure 8-3, V_{CANL} = 40 V, CANH = open, TXD = 0 V			100	mA
$I_{OS(REC)}$	Short circuit steady-state output current recessive		See Figure 7-10 and Figure 8-3 –27 V ≤ V_{BUS} ≤ 32 V, V_{BUS} = CANH = CANL, TXD = V_{IO}	–5		5	mA
$V_{O(STB)}$	Bus output voltage Standby mode	CANH	STB = V_{CC} or V_{IO}, R_L = open, R_{CM} = open	–0.1	0	0.1	V
		CANL		–0.1	0	0.1	V
		CANH - CANL		–0.2	0	0.2	V
Receiver Electrical Characteristics							
V_{CM}	Common mode range Normal and Silent modes		See Figure 7-3 and Table 8-5	-30		30	V
V_{IT}	Input threshold voltage Normal and Silent modes		See Figure 7-3 and Table 8-5, V_{CM} ≤ ±20 V	500		900	mV
			See Figure 7-3 and Table 8-5, V_{CM} ≤ ±30 V	400		1000	mV
V_{REC}	Receiver recessive voltage		See Figure 7-3 and Table 8-5 Normal or Silent mode, V_{CM} = ±20 V	-3		0.5	V
V_{DOM}	Receiver dominant voltage			0.9		8	V
V_{HYS}	Hysteresis voltage for input threshold Normal and Silent modes		See Figure 7-3 and Table 8-5		120		mV
$V_{IT(Sleep)}$	Input threshold Sleep mode		See Figure 7-3 and Table 8-5; V_{CM} = ± 12 V	400		1150	mV
$V_{REC(Sleep)}$	Receiver recessive voltage Sleep mode			-3		0.4	V
$V_{DOM(Sleep)}$	Receiver dominant voltage Sleep mode			1.15		8	V
V_{CM}	Common mode range Standby, Go-to-Sleep and Sleep modes		See Figure 7-3 and Table 8-5	-12		12	V
$I_{IOFF(LKG)}$	Power-off (unpowered) bus input leakage current		CANH = CANL = 5 V, V_{CC} = GND, V_{IO} = GND, V_{SUP} = 0 V			4.8	µA
C_I	Input capacitance to ground (CANH or CANL)		TXD = V_{CC}, V_{IO} = V_{CC} [4]		24	30	pF
C_{ID}	Differential input capacitance (CANH or CANL)				12	15	pF
R_{ID}	Differential input resistance		TXD = V_{CC} = V_{IO} = 5 V, Normal mode; -30 ≤ V_{CM} ≤ +30V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)			15		40	kΩ

6.7 Electrical Characteristics (continued)

Over recommended operating conditions with T_A = –55°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$R_{IN(M)}$	Input resistance matching: [1 – $R_{IN(CANH)}$ / $R_{IN(CANL)}$] × 100%	$V_{(CANH)}$ = $V_{(CANL)}$ = 5 V	–2%		2%	
R_{CBF}	Valid differential load impedance range for bus fault circuitry	R_{CM} = R_L, C_L = open	45		70	Ω
TXD TERMINAL (CAN TRANSMIT DATA INPUT)						
V_{IH}	High level input voltage		0.7 V_{IO}			V
V_{IL}	Low level input voltage				0.3 V_{IO}	V
I_{IH}	High level input leakage current	TXD = V_{CC} = V_{IO} = 5.5 V	–2.5	0	1	µA
I_{IL}	Low level input leakage current	TXD = 0 V, V_{CC} = V_{IO} = 5.5 V	–100		–2.5	µA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V, V_{CC} = V_{IO} = 0 V	–1	0	1	µA
C_I	Input capacitance	V_{IN} = 0.4 x sin(2 x π x 2 x 10^6 x t) + 2.5 V		5		pF
RXD TERMINAL (CAN RECEIVE DATA OUTPUT)						
V_{OH}	High level output voltage	See Figure 7-3, I_O = –2 mA.	0.8 V_{IO}			V
V_{OL}	Low level output voltage	See Figure 7-3, I_O = –2 mA.			0.2 V_{IO}	V
nFAULT TERMINAL (FAULT AND STATUS OUTPUT)						
V_{OH}	High level output voltage	See Figure 7-1, I_O = –2 mA.	0.8 V_{IO}			V
V_{OL}	Low level output voltage	See Figure 7-1 I_O = 2 mA.			0.2 V_{IO}	V
nSTB TERMINAL (STANDBY MODE INPUT)						
V_{IH}	High level input voltage		0.7 V_{IO}			V
V_{IL}	Low level input voltage				0.3 V_{IO}	V
I_{IH}	High level input leakage current	nSTB = V_{CC} = V_{IO} = 5.5 V	0.5		10	µA
I_{IL}	Low level input leakage current	nSTB = 0 V, V_{CC} = V_{IO} = 5.5 V	–1		1	µA
$I_{LKG(OFF)}$	Unpowered leakage current	nSTB = 5.5 V, V_{CC} = 0 V, V_{IO} = 0 V	–1	0	1	µA
EN TERMINAL (ENABLE MODE INPUT)						
V_{IH}	High level input voltage		0.7 V_{IO}			V
V_{IL}	Low level input voltage				0.3 V_{IO}	V
I_{IH}	High level input leakage current	EN = V_{CC} = V_{IO} = 5.5 V	0.5		10	µA
I_{IL}	Low level input leakage current	EN = 0 V, V_{CC} = V_{IO} = 5.5 V	–1		1	µA
$I_{LKG(OFF)}$	Unpowered leakage current	EN = 5.5 V, V_{CC} = 0 V, V_{IO} = 0 V	–1	0	1	µA
INH TERMINAL (INHIBIT OUTPUT)						
ΔV_H	High level voltage drop INH with respect to V_{SUP}	I_{INH} = –0.5 mA		0.5	1	V
$I_{LKG(INH)}$	Leakage current	INH = 0 V, Sleep Mode	-5		5	µA
Wake TERMINAL (WAKE INPUT)						
V_{IH}	High level input voltage	Standby and Sleep Mode	V_{SUP} - 1.9			V
V_{IL}	Low level input voltage	Standby and Sleep Mode			V_{SUP} - 3.5	V
I_{IH}	High level input current(5)	WAKE = V_{SUP} – 1 V	–25	–15		µA
I_{IL}	Low level input current(5)	WAKE = 1 V		15	25	µA

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V, V_{IO} = 3.3 V, and R_L = 60 Ω. Unless otherwise noted.
(2) The recessive bus voltage is the same if the device is in Normal mode with the nSTB and EN terminals high or if the device is in Silent mode with the nSTB terminal high and EN terminal low.
(3) The bus output voltage symmetry, V_{SYM}, is measured using R_{TERM} / 2 = 30 Ω and C_{SPLIT} = 4.7 nF as shown in Figure 9-4
(4) Specified by design and verified during product validation using the ISO 11898-2 method.
(5) To minimize system level current consumption, the WAKE automatically configures itself based on the applied voltage to have either an internal pull-up or pull-down current source. A high level input results in an internal pull-up and a low level input results in an internal pull-down. For more information, refer to Section 8.4.6.2.

6.8 Switching Characteristics

Over recommended operating conditions with T_A = -55°C to 125°C (unless otherwise noted)

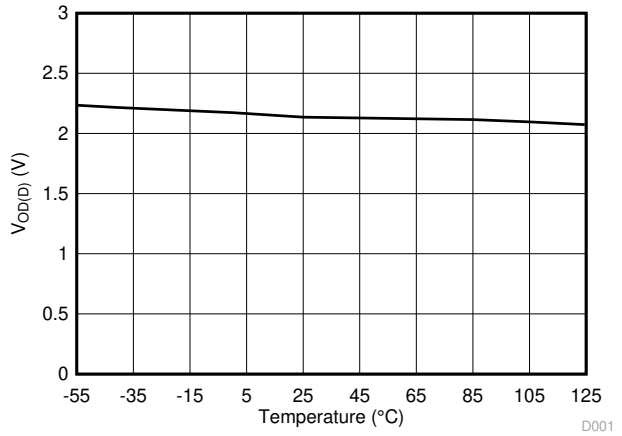
PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
DRIVER SWITCHING CHARACTERISTICS						
t_{pHR}	Propagation delay time, high TXD to driver recessive	See Figure 7-2, Normal mode. R_L = 60 Ω, C_L = 100 pF, R_{CM} = open		50		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant			40		ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHR} - t_{pLD} \rvert$)			10		ns
t_R	Differential output signal rise time			45		ns
t_F	Differential output signal fall time			45		ns
t_{TXD_DTO}	Dominant time out	See Figure 7-9, R_L = 60 Ω, C_L = open	1.2		3.8	ms
RECEIVER SWITCHING CHARACTERISTICS						
t_{pRH}	Propagation delay time, bus recessive input to high RXD	See Figure 7-3 $C_{L(RXD)}$ = 15 pF		50		ns
t_{pDL}	Propagation delay time, bus dominant input to RXD low output			50		ns
t_R	Output signal rise time (RXD)			8		ns
t_F	Output signal fall time (RXD)			8		ns
t_{BUS_DOM}	Dominant time out	See Figure 17, R_L = 60 Ω, C_L = open	1.3		3.8	ms
t_{CBF}	Bus fault detection time	45 Ω ≤ R_{CM} ≤ 70 Ω, C_L = open	1.9			µs
Wake Terminal (Wake input)						
t_{WAKE_HT}	WAKE hold time	See Figure 7-12 and Figure 7-13 Time required for LWU from a high to low or low to high on WAKE	5		50	µs
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	See Figure 7-5, Normal mode, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		100	160	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive			110	175	ns
t_{MODE1}	Mode change time	See Figure 7-4 and Figure 7-5, Mode change time for leaving Sleep mode to entering normal and silent mode after V_{CC} and V_{IO} have crossed UV thresholds			20	µs
t_{MODE2}	Mode change time	Mode changes between Normal, Silent and Standby modes, and Sleep to Standby mode transition			10	µs
$t_{UV\_RE-ENABLE}$	Re-enable time after under voltage event	Time for device to return to normal operation from UV_{VCC} or UV_{VIO} under voltage event			200	µs
t_{Power_Up}	Power up time on V_{SUP}	See Figure 7-11		250		µs
t_{WK_FILTER}	Bus time to meet filtered bus requirements for wake up request	See Figure 8-5	0.5		1.8	µs
$t_{WK\_TIMEOUT}$	Bus Wake-up timeout value	See Figure 8-5	0.5		2	ms
t_{UV}	Undervoltage filter time for V_{IO} and V_{CC}	V_{IO} ≤ UV_{VIO} or V_{CC} < UV_{VCC}	159		340	ms
$t_{Go\_To\_Sleep}$	Minimum hold time for transition to sleep mode	EN = H and nSTB = L	5		50	µs
FD Timing Parameters						

6.8 Switching Characteristics (continued)

Over recommended operating conditions with T_A = -55°C to 125°C (unless otherwise noted)

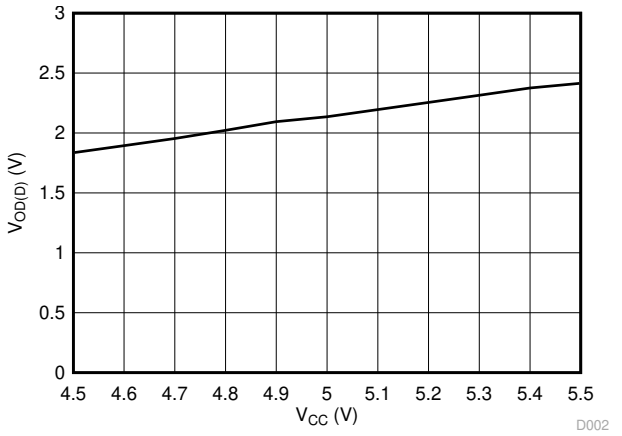
PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns, all devices	Normal mode, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	435		530	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns, G device variants only		155		210	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns, all devices		400		550	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns, G device variants only		120		220	ns
Δt_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns, all devices		-65		40	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns, G device variants only		-45		15	ns

6.9 Typical Characteristics



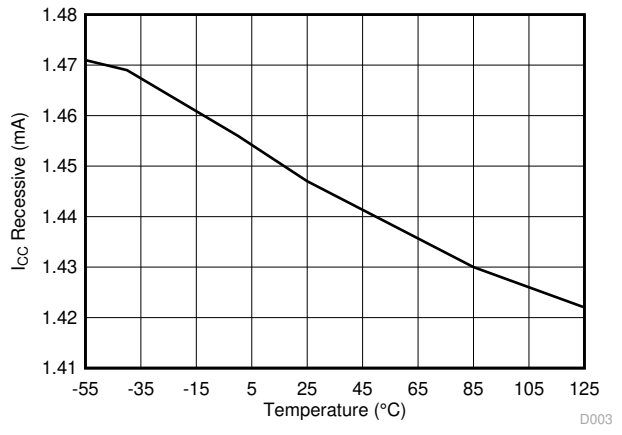
V_{CC} = 5 V | V_{IO} = 3.3 V | R_L = 60 Ω
C_L = Open | RCM = Open | STB = 0 V

Figure 6-1. $V_{OD(D)}$ Over Temperature



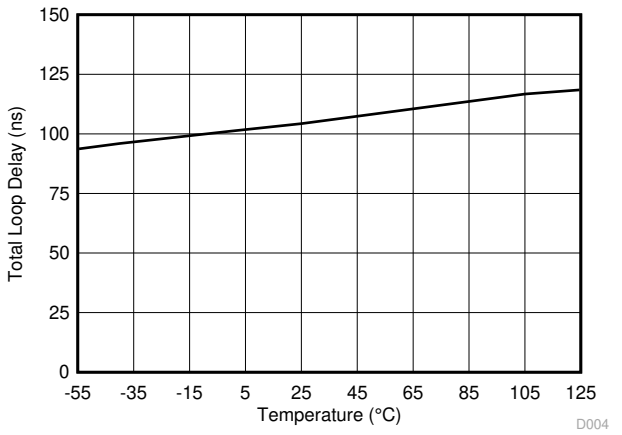
V_{IO} = 5 V | STB = 0 V | R_L = 60 Ω
C_L = Open | RCM = Open | Temp = 25°C

Figure 6-2. $V_{OD(D)}$ Over V_{CC}



V_{CC} = 5 V | V_{IO} = 3.3 V | R_L = 60 Ω
C_L = Open | RCM = Open | STB = 0 V

Figure 6-3. I_{CC} Recessive Over Temperature



V_{CC} = 5 V | V_{IO} = 3.3 V | R_L = 60 Ω
C_L = 100 pF | C_{L_RXD} = 15 pF | STB = 0 V

Figure 6-4. Total Loop Delay Over Temperature

7 Parameter Measurement Information

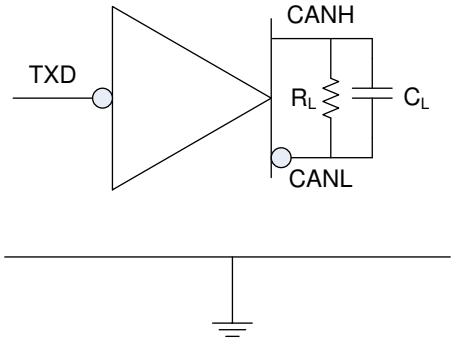


Figure 7-1. Supply Test Circuit

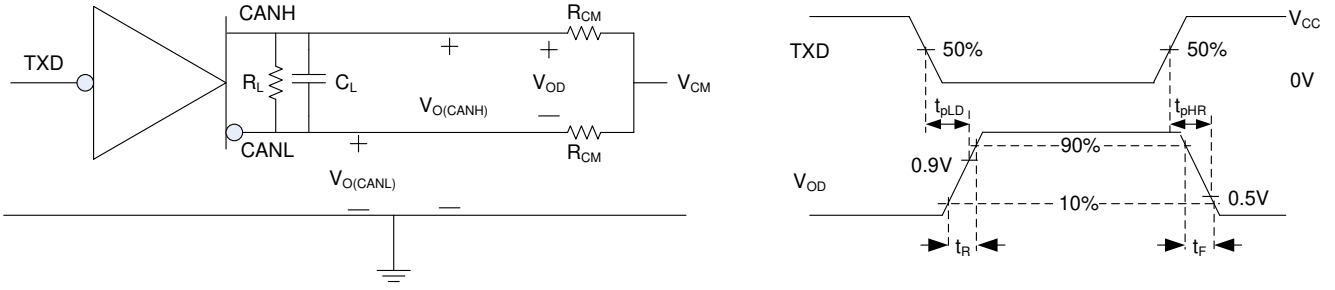


Figure 7-2. Driver Test Circuit and Measurement

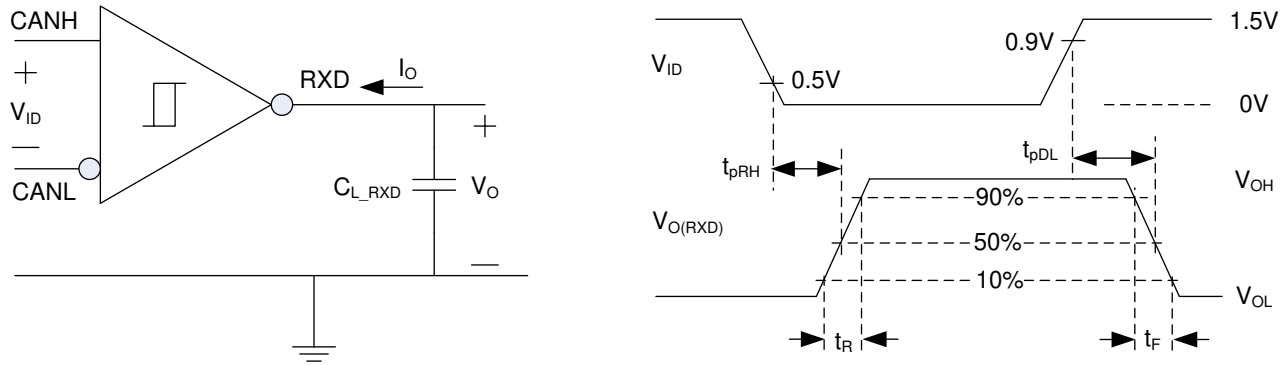


Figure 7-3. Receiver Test Circuit and Measurement

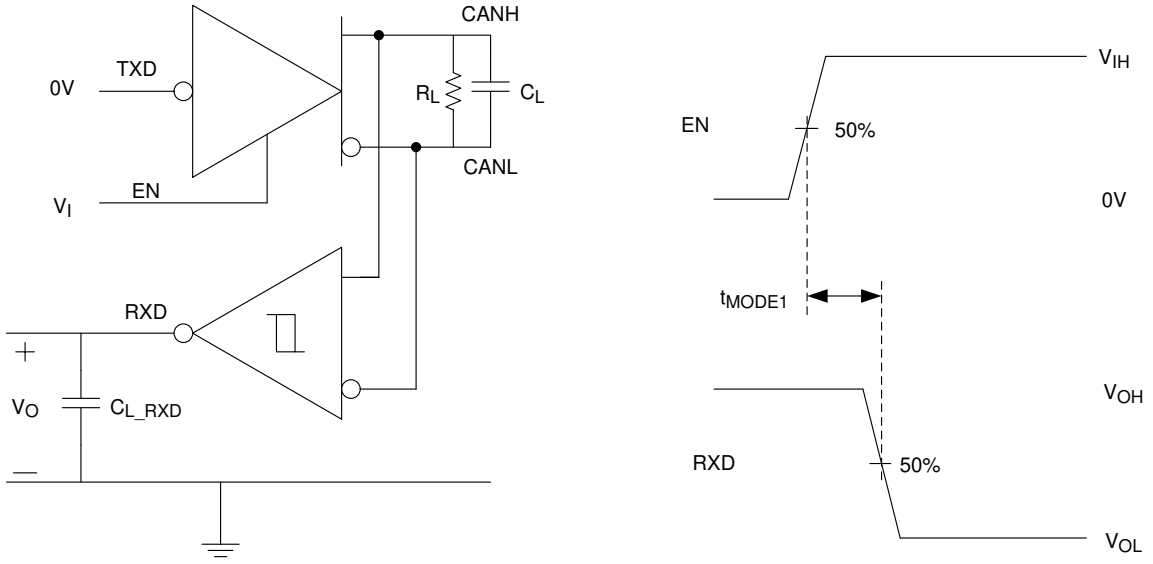


Figure 7-4. t_{MODE1} Test Circuit and Measurement, Silent Mode to Normal Mode

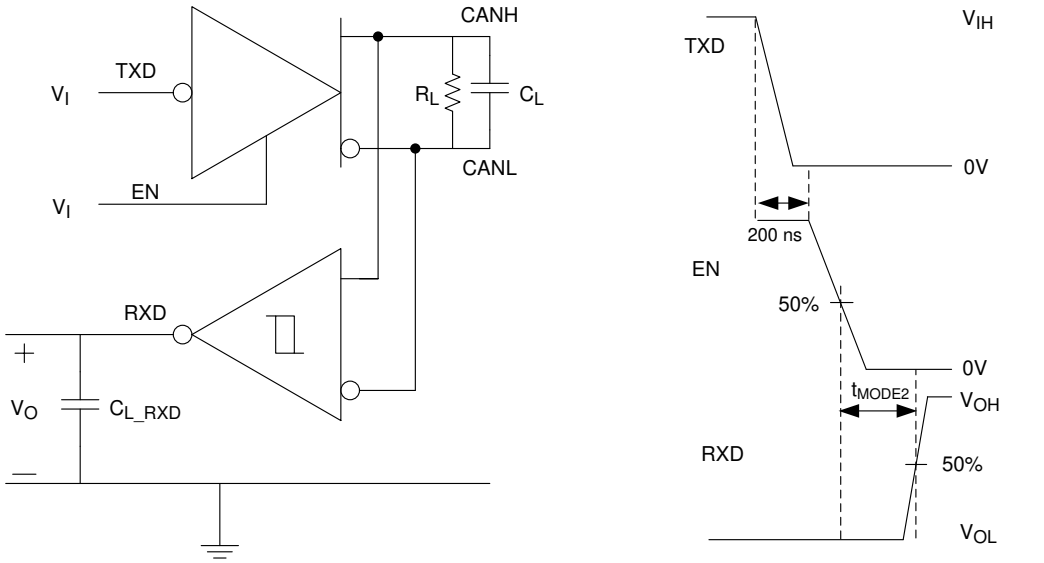


Figure 7-5. t_{MODE2} Test Circuit and Measurement, Normal Mode to Silent Mode

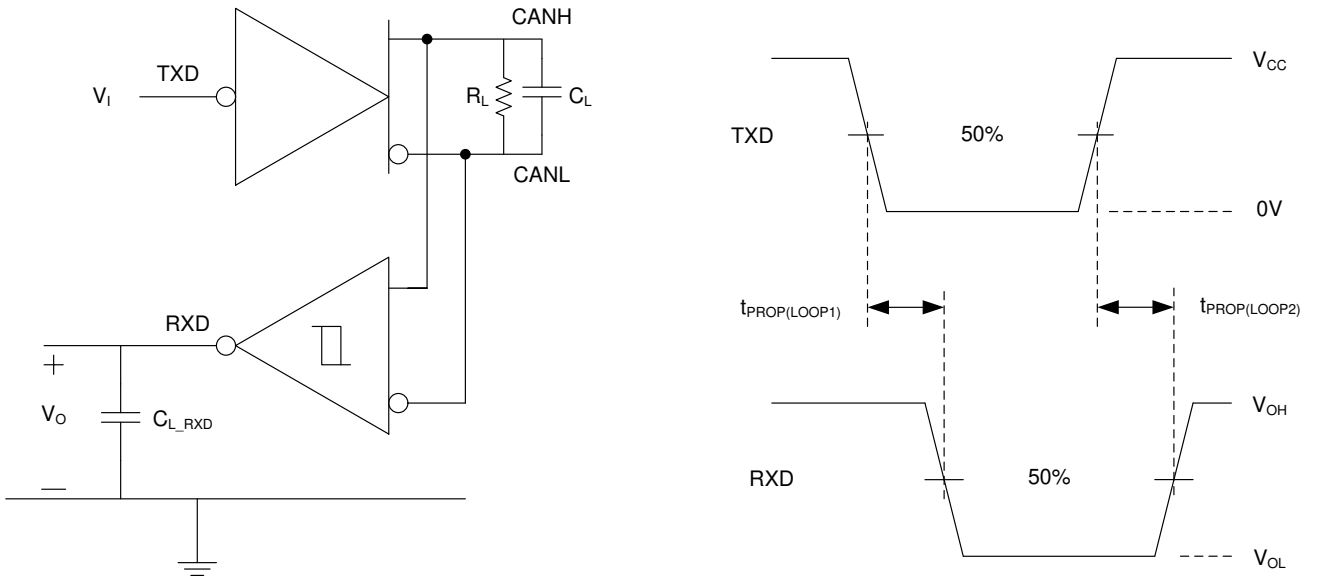


Figure 7-6. $t_{PROP(LOOP)}$ Test Circuit and Measurement

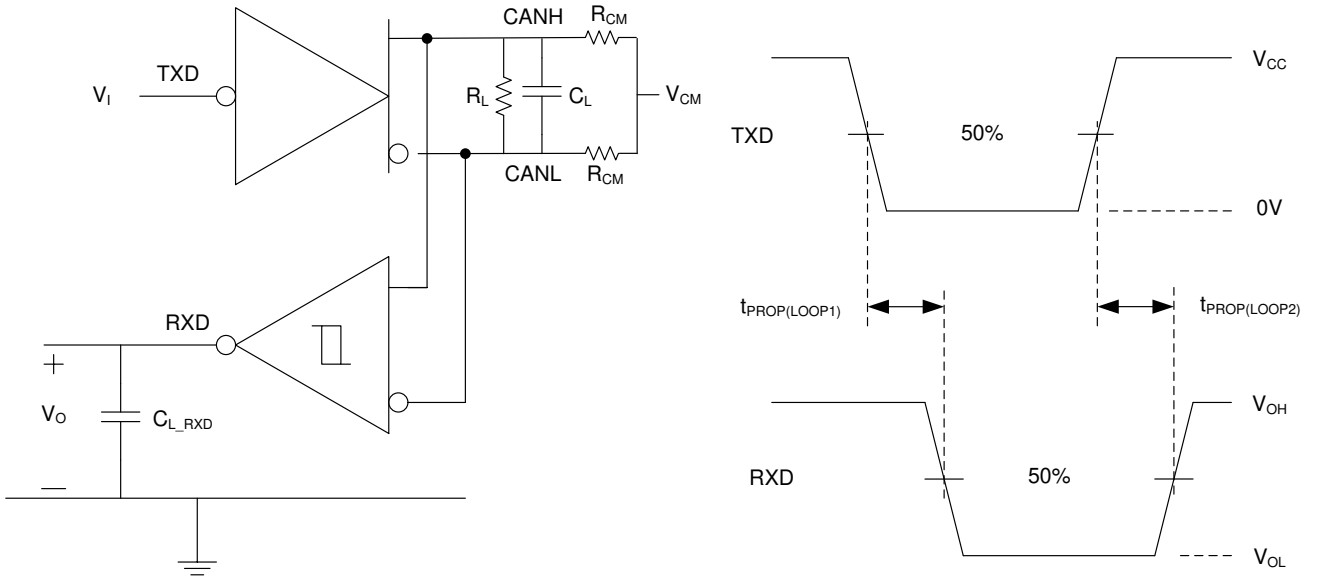


Figure 7-7. $t_{PROP(LOOP)}$ Test Circuit and Measurement with CM Range

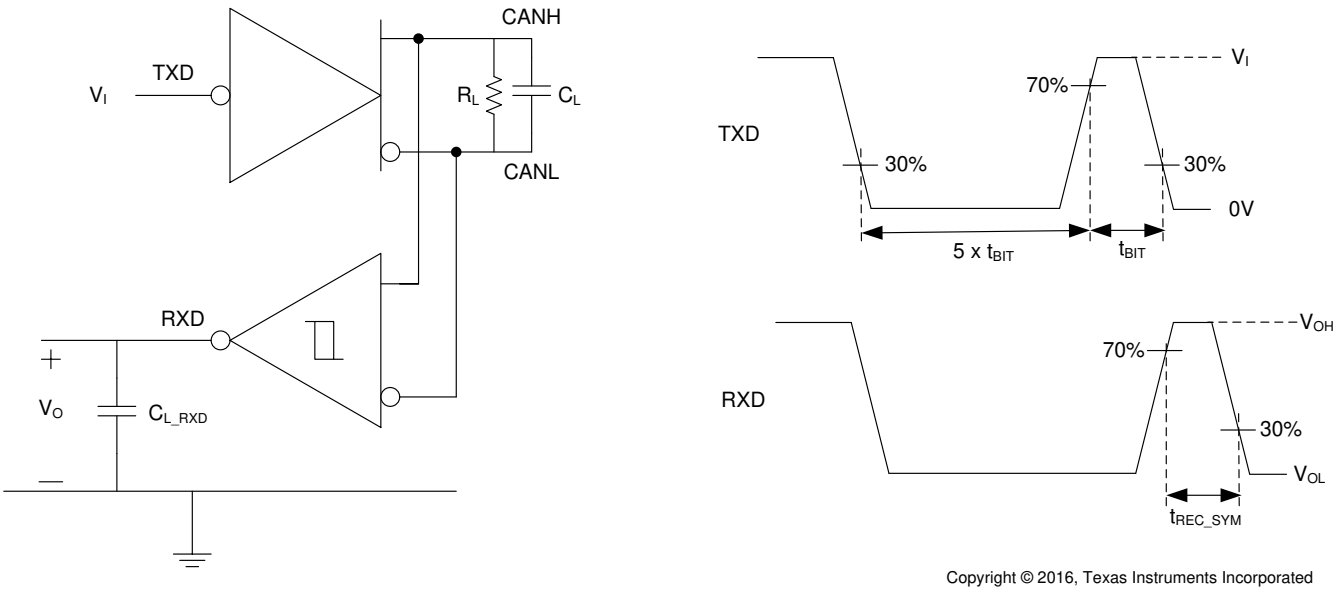


Figure 7-8. Loop Delay Symmetry Test Circuit and Measurement

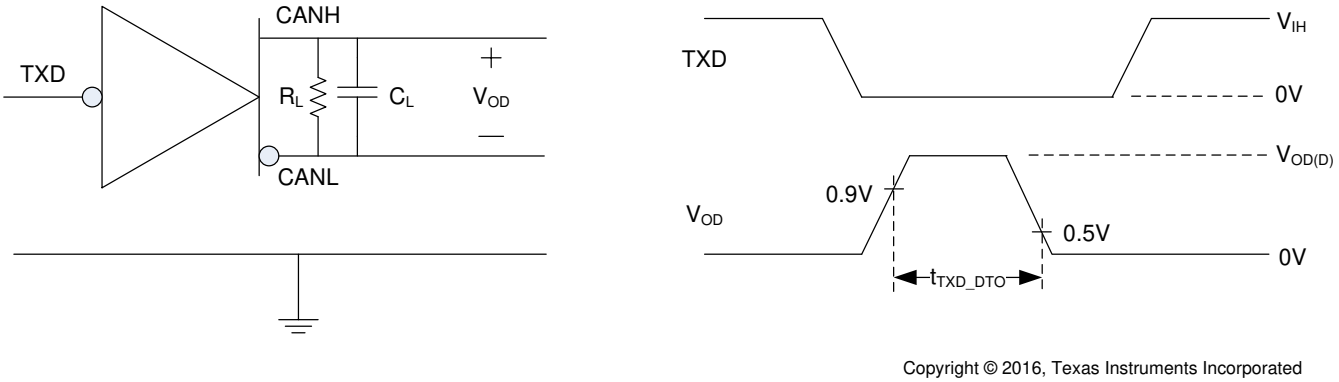


Figure 7-9. TXD Dominant Timeout Test Circuit and Measurement

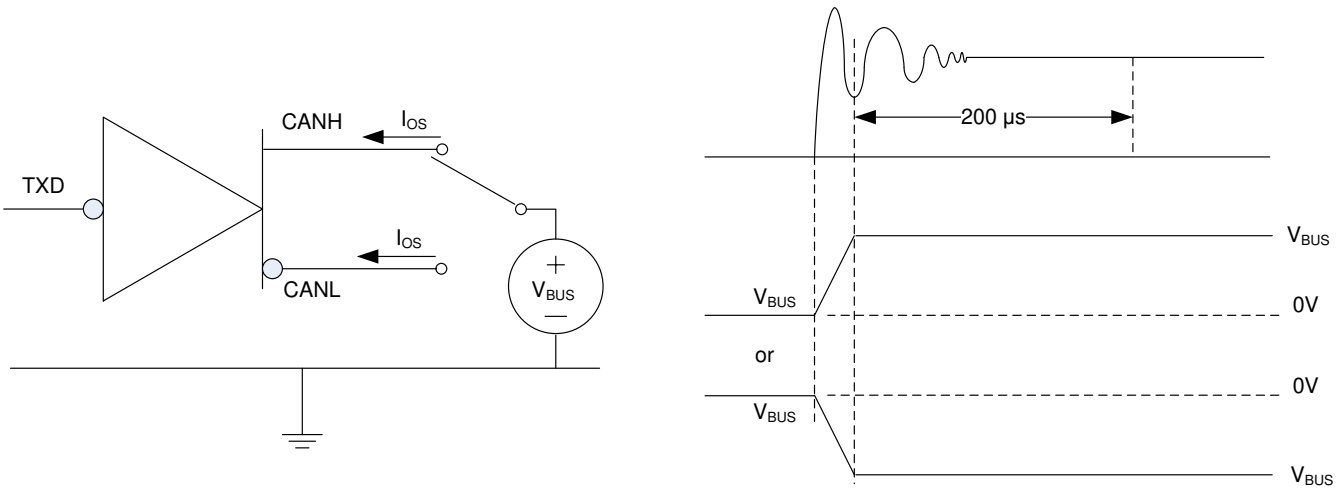


Figure 7-10. Driver Short-Circuit Current Test and Measurement

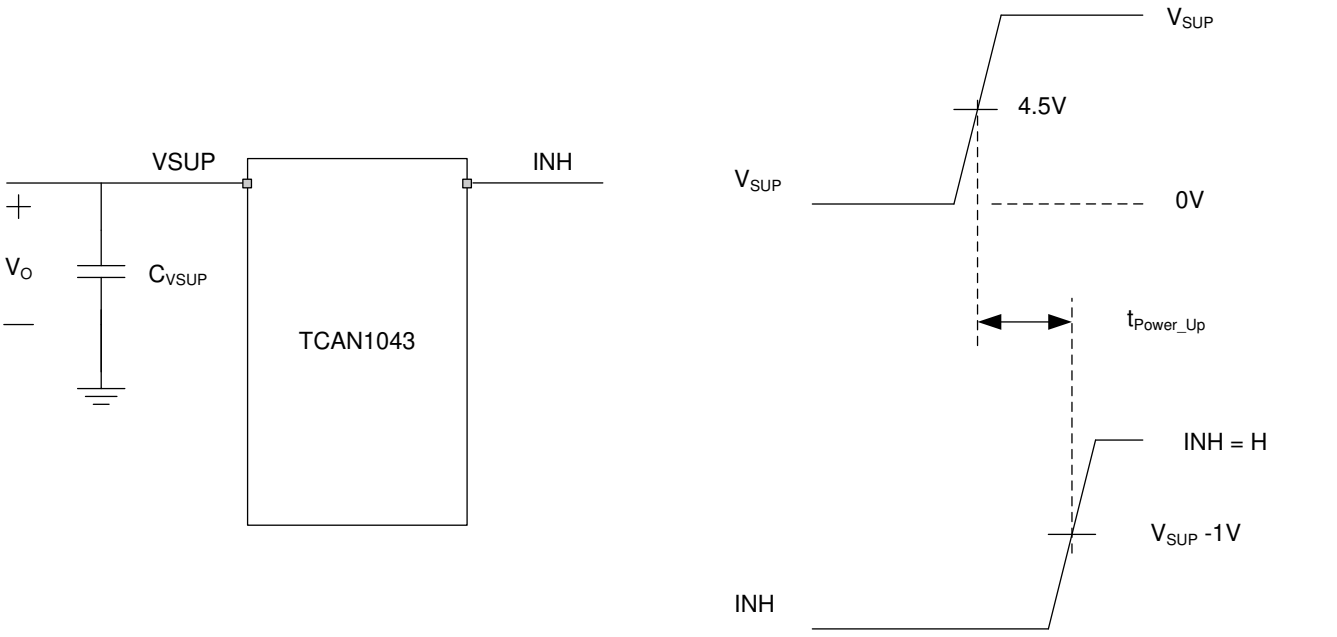


Figure 7-11. t_{Power_Up} Timing Measurement

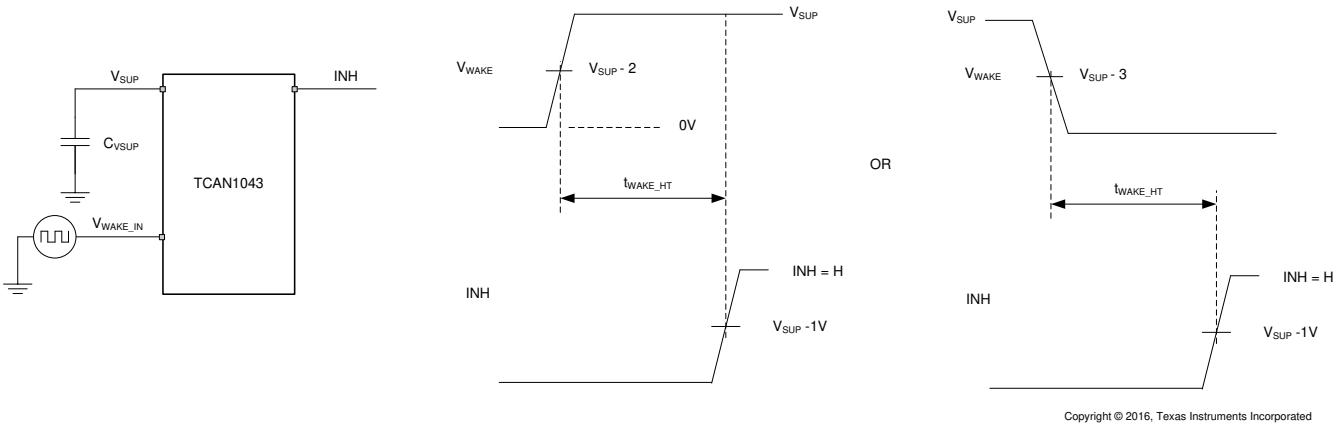


Figure 7-12. t_{WAKE_HT} While Monitoring INH Output

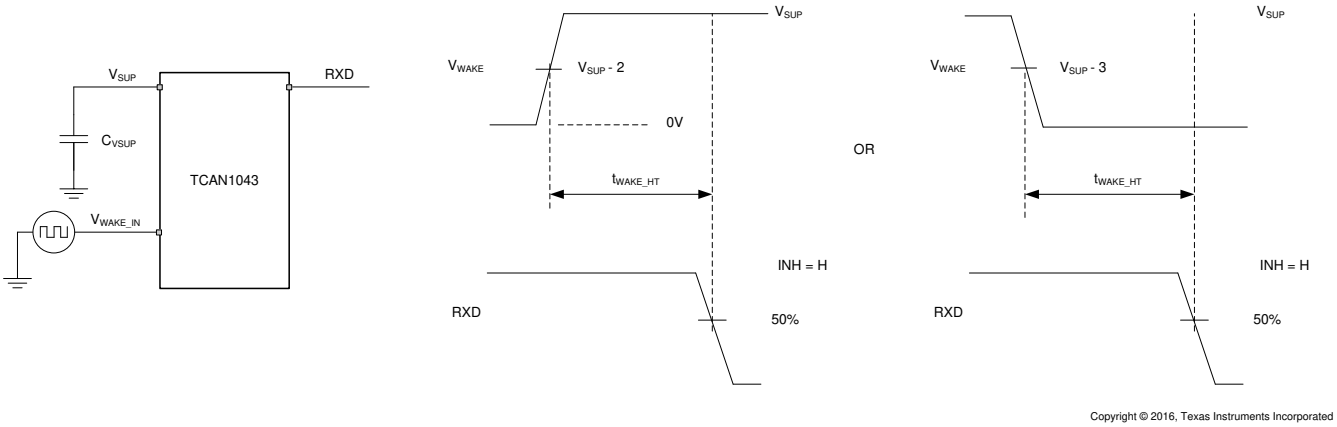


Figure 7-13. t_{WAKE_HT} While Monitoring RXD Output

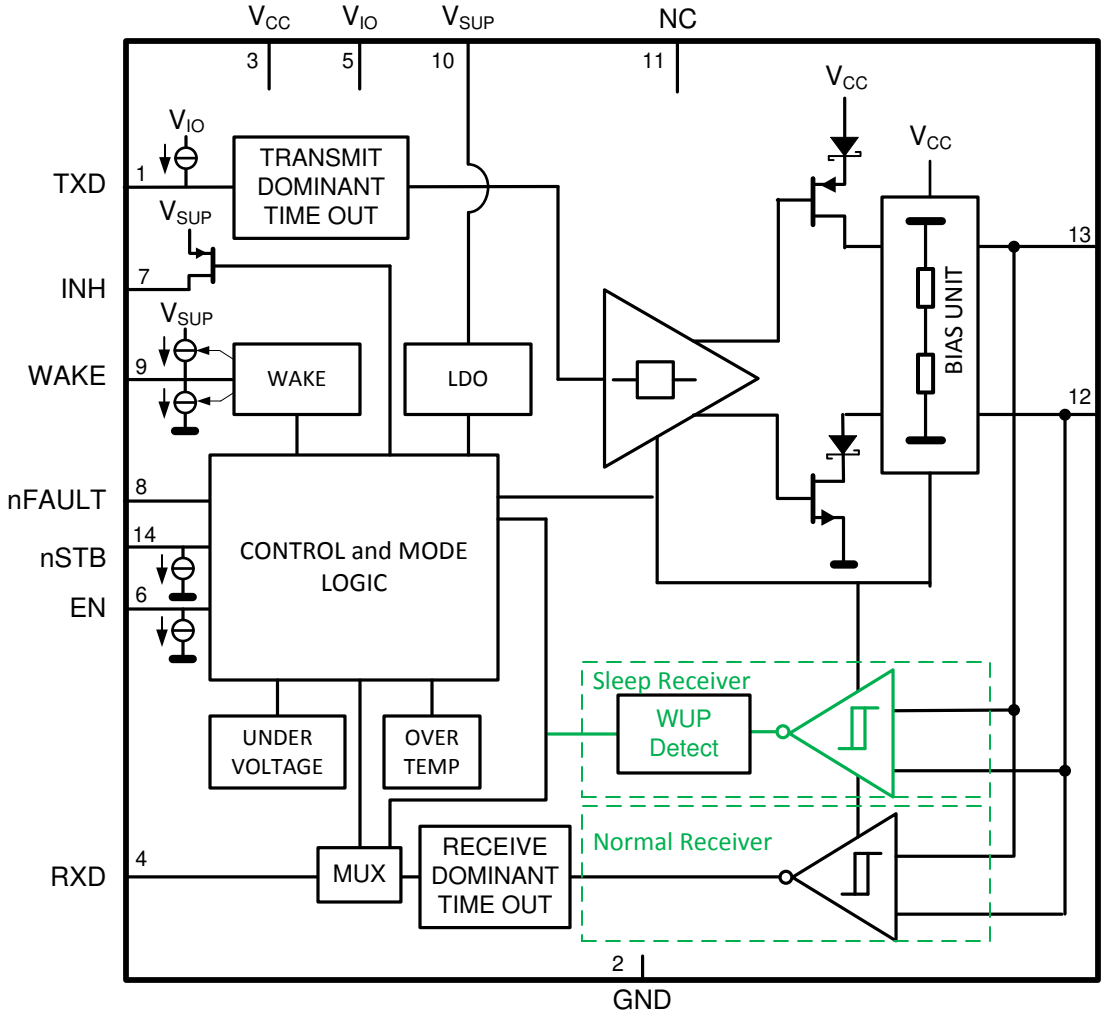
8 Detailed Description

8.1 Overview

The TCAN1043xx-Q1 meets or exceeds the specifications of the ISO 11898-2 (2016) High Speed CAN (Controller Area Network) physical layer standard. The device has been certified to the requirements of ISO11898-2/5 according to the GIFT/ICT High Speed CAN test specification.

This device provides CAN transceiver differential transmit capability to the bus and differential receive capability from the bus. The device includes many protection features providing device and CAN bus robustness. All of the devices are available to support CAN and CAN FD (Flexible Data Rate) up to 2Mbps while the G version of the device support CAN and CAN FD data rates up to 5Mbps.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Internal and External Indicator Flags (nFAULT and RXD)

The following device status indicator flags are implemented to allow for the MCU to determine the status of the device and the system. In addition to faults, the nFAULT terminal also signals wake up requests and a *cold* power-up sequence on the V_{SUP} battery terminal so the system can do any diagnostics or cold booting sequence necessary. The RXD terminal indicates wake up request and the faults are multiplexed (ORed) to the nFAULT output.

Table 8-1. Device Status Indicator Flags

EVENT	FLAG NAME	CAUSE	INDICATORS(1)	FLAG IS CLEARED	COMMENT
Power-up	PWRON	Power up on VSUP and any return of VSUP after it has been below UV_{VSUP}	nFAULT = L upon entering Silent mode from Standby, Go-to-Sleep, or Sleep mode	After transition to normal mode	
Wake-up Request	WAKERQ(2)	Wake up event on CAN bus, state transition on WAKE pin, or initial power up	nFAULT = RXD = L after wake up in standby mode, go-to-sleep mode, and sleep mode	After transition to normal mode, or either a UV_{VCC} or UV_{VIO} event	Wake up request can only be set from standby, Go-to-sleep, or sleep mode. Resets timers for UV_{VCC} or UV_{VIO}
Wake-up Source Recognition(3)	WAKESR	Wake up event on CAN bus, state transition on WAKE pin, initial power up	Available upon entering normal mode(4) , nFAULT = L indicates wake from WAKE terminal, nFAULT = H indicates wake from CAN bus	After four recessive to dominant edges on TXD in normal mode,leaving normal mode, or either a UV_{VCC} or UV_{VIO} event	A LWU source flag is set on initial power up
Under voltage	UVVCC	Under voltage V_{CC}	Not externally indicated	VC_C returns, or Wake-up request occurs	
	UVVIO	Under voltage V_{IO}	Not externally indicated	V_{IO} returns, or Wake-up request occurs	
	UVVSUP	Under voltage V_{SUP}	Not externally indicated	V_{SUP} returns	V_{SUP} undervoltage event triggers the PWRON and WAKERQ flags upon return of VSUP
CAN Bus Failures	CBF	CANH shorted to GND, V_{CC}, V_{SUP} or CANL shorted to GND, V_{CC}, V_{SUP}	nFAULT = L in Normal mode only(5)	Upon leaving Normal mode, or if no CAN bus fault is detected for four consecutive dominant to recessive transitions of the TXD pin while in normal mode.	Failure must persist for four consecutive dominant to recessive transitions
Local Faults	TXDDTO	TXD Dominant Time Out, dominant (low) signal for $t \geq t_{TXD\_DTO}$	nFAULT = L upon entering Silent mode from Normal mode	RXD = L and TXD = H, or upon transitioning into Normal, Standby, Go-to-Sleep, or Sleep modes	CAN driver remains disabled until the TXDDTO is cleared
	TXDRXD	TXD and RXD pins are shorted together for $t \geq t_{TXD\_DTO}$			CAN driver remains disabled until the TXDRXD is cleared
	CANDOM	CAN bus dominant fault, when dominant bus signal received for $t \geq t_{BUS\_DOM}$		RXD = H, or upon transitioning into Normal, Standby, Go-to-Sleep, or Sleep modes	Driver remains enabled
	TSD	Thermal Shutdown, junction temperature $\geq T_{TSD}$		T_J drops below t_{TSD} and either RXD = L and TXD = H, or upon transitioning into Normal, Standby, Go-to-Sleep, or Sleep modes	CAN driver remains disabled until the TSD is cleared

(1) V_{IO} and V_{SUP} are present.
(2) Transitions to Go-to-sleep mode is blocked until WAKERQ flag is cleared.
(3) Wake-up source recognition reflects the first wake up source. If additional wake-up. events occur the source still indicates the original wake up source.
(4) Indicator is only available in normal mode until the flag is cleared.
(5) CAN Bus failure flag is indicated after four recessive-to-dominant edges on TXD.

8.3.2 Power-Up Flag (PWRON)

This is an internal and external flag that is set and controls the power up state of the device. The device powers on to standby mode with the PWRON flag set after V_{SUP} has cleared the under voltage lock out for V_{SUP}, UV_{VSUP}.

8.3.3 Wake-Up Request Flag (WAKERQ)

This is an internal and external flag that can be set in standby, go-to-sleep, or sleep mode. This flag is set when either a valid local wake up (LWU) request occurs, or a valid remote wake request occurs, or on power up on V_{SUP}. The setting of this flag clears t_{UV} timer for the UV_{VCC} or UV_{VIO}. This flag is cleared upon entering normal mode or during a under voltage event on V_{CC} or V_{IO}.

8.3.4 Wake-Up Source Recognition Flag (WAKESR)

This flag is an internal and external flag that is set high or low after a valid local wake up (LWU) request occurs, or a valid remote wake request occurs. This flag is only available in Normal mode before four recessive to dominant transitions occur on TXD. If the nFAULT pin is high after entering normal mode, this indicates that a remote wake request was received. If the nFAULT output is low after entering Normal mode, this indicates that a local wake up event occurred. Upon power up on V_{SUP}, or after and under voltage event on V_{SUP}, the local wake up request is indicated on nFAULT.

8.3.5 Undervoltage Fault Flags

The TCAN1043xx-Q1 device comes with undervoltage detection circuits on all three supply terminals: V_{SUP}, V_{CC}, and V_{IO}. These flags are internal flags and are not indicated on the nFAULT terminal.

8.3.5.1 Undervoltage on V_{CC} Fault

This internal flag is set when the voltage on V_{CC} drops below the undervoltage detection voltage threshold, UV_{VCC}, for longer than the undervoltage filter time, t_{UV}.

8.3.5.2 Undervoltage on V_{IO} Fault

This internal flag is set when the voltage on V_{IO} drops below the undervoltage detection voltage threshold, UV_{VIO}, for longer than the undervoltage filter time, t_{UV}.

8.3.5.3 Undervoltage on V_{SUP} Fault

This internal flag is set when the voltage on V_{SUP} drops below the undervoltage detection voltage threshold, UV_{VSUP}. While this flag is not externally indicated, the PWRON and WAKERQ flags are set once the V_{SUP} supply returns.

8.3.6 CAN Bus Failure Fault Flag

The TCAN1043xx-Q1 devices are able to detect the following six faults that can occur on the CANH and CANL bus terminals. These faults are only detected in Normal mode, and are only indicated via the nFAULT terminal while in Normal mode.

1. CANH bus pin shorted V_{SUP}
2. CANH bus pin shorted V_{CC}
3. CANH bus pin shorted GND
4. CANL bus pin shorted V_{SUP}
5. CANL bus pin shorted V_{CC}
6. CANL bus pin shorted GND

These failures are detected while transmitting a dominant signal on the CAN bus. If one of these fault conditions persists for four consecutive dominant bit transmissions, the nFAULT indicates a CAN bus failure flag in Normal mode by driving the nFAULT pin low. The CAN bus driver remains active.

The bus fault failure circuitry is able to detect bus faults for a range of differential resistance loads (R_{CBF}), for data rates from 250kbps to 1Mbps, and within nominal temperature conditions (25°C to 60°C). Outside of these

ranges, the CAN bus fault detection circuitry becomes less reliable, potentially reporting CAN bus faults when there are none present.

8.3.7 Local Faults

Local faults are detected in both Normal mode and Silent mode, but are only indicated via the nFAULT pin when transitioned form Normal mode to Silent mode. All other mode transitions clear the local fault flag indicators.

8.3.7.1 TXD Dominant Timeout (TXD DTO)

During Normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time out period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time out constant of the circuit, t_{TXD_DTO}, expires, the CAN driver is disabled. This keeps the bus free for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on the TXD terminal, thus clearing the dominant time out. The receiver and RXD terminal reflects what is on the CAN bus and the bus terminals is biased to recessive level during a TXD DTO. This fault is indicated via the TXDDTO flag shown on the nFAULT terminal.

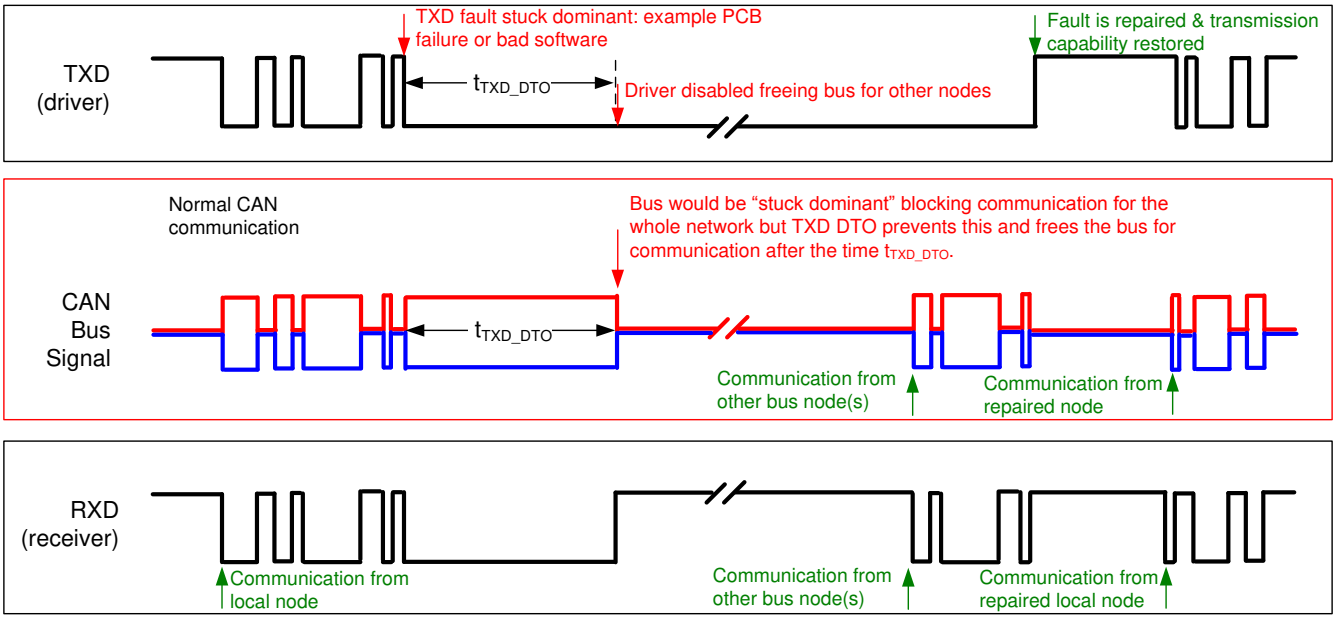


Figure 8-1. Example Timing Diagram for TXD DTO

Note

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated by: Minimum Data Rate = 11 bits / t_{TXD_DTO} = 11 bits / 1.2 ms = 9.2 kbps.

8.3.7.2 TXD Shorted to RXD Fault

The TXDRXD flag is set if the device detects that the TXD and RXD lines have been shorted together for t ≥t_{TXD_DTO}. This fault is then indicated via the nFAULT terminal. The CAN driver is disabled until the TXDRXD fault is cleared.

This fault is only indicated in Normal mode and Silent mode.

8.3.7.3 CAN Bus Dominant Fault

The CAN bus dominant fault detects if the CAN bus is stuck in a permanent dominant (low) state. This fault is detected when the device detects a dominant on the bus for time ≥ t_{BUS_DOM}. This fault is then indicated via the CANDOM flag shown on the nFAULT terminal.

This fault is only indicated on the nFAULT pin in Silent mode. This fault can also be seen on the RXD pin as a dominant pulse for a time ≥ t_{BUS_DOM}.

8.3.7.4 Thermal Shutdown (TSD)

If the junction temperature of the device exceeds the thermal shut down threshold, the device turns off the CAN driver circuits thus blocking the TXD to the bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below the thermal shutdown temperature of the device. If the fault condition that caused the thermal shutdown is still present, the temperature may rise again causing the device to reenter thermal shut down. Prolonged operation with thermal shutdown conditions may affect device reliability. The thermal shutdown circuit includes hysteresis to avoid oscillation of the driver output. This fault is indicated via the TSD flag shown on the nFAULT terminal.

8.3.7.5 RXD Recessive Fault

The RXD recessive fault detects if the RXD terminal is stuck (clamped) in a permanent recessive state. This fault is detected when the device transmits four dominant bits to the bus via TXD but the RXD output does not follow. This fault is then indicated via the RXDREC flag shown on the nFAULT terminal.

8.3.7.6 Undervoltage Lockout (UVLO)

The supply terminals have under voltage detection which puts the device in protected mode if one of the supply rails drop below the threshold voltage. This protects the bus and system during an under voltage event on either V_{SUP}, V_{CC} or V_{IO} supply terminals. These faults are internal fault flags and are not indicated via the nFAULT terminal.

During an undervoltage event on V_{CC} or V_{IO} the device goes into protected mode and the driver is disabled. After the UV timer expires, the device transitions into sleep mode and the INH pin goes into a high impedance state. In the event of a UV on V_{IO} where the mode pins are no longer driven, the device transitions into standby mode (due to internal fail safe biasing on the NSTB and EN pins) until the UV timer expires and the device transitions into sleep mode.

The V_{CC} and V_{IO} undervoltage detection circuits share the same timer. Therefore, if an undervoltage on one supply occurs and the timers starts, and then during the undervoltage the other supply has an undervoltage event before the first supply recovers the timer does not reset.

Once an under voltage condition is cleared and the supplies have returned to valid levels the device typically needs 200 µs to transition to normal operation.

8.3.7.7 Unpowered Device

The device is designed to be an "ideal passive" or “no load” to the CAN bus when unpowered. The bus terminals (CANH, CANL) have low leakage currents when the device is un-powered so the terminals do not load down the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation.

Logic terminals also have low leakage currents when the device is un-powered, so the terminals do not load down other circuits which can remain powered.

8.3.7.8 Floating Terminals

These devices have internal pull ups on critical terminals to place the device into known states if the terminals float. See Table 8-2 for details on terminal bias conditions.

Table 8-2. Terminal Failsafe Biasing

TERMINAL	PULL UP or PULL DOWN	COMMENT
TXD	Pull up	Weakly biases TXD toward recessive to prevent bus blockage or TXD DTO triggering
nSTB	Pull down	Weakly biases nSTB terminal towards low power Standby mode to prevent excessive system power
EN	Pull down	Weakly biases EN terminal towards low power mode to prevent excessive system power

Note

The internal bias should not be relied on by design, especially in noisy environments but should be considered a fall back protection. Special care needs to be taken when the device is used with MCUs using open drain outputs. TXD is weakly internally pulled up. The TXD pull up strength and CAN bit timing require special consideration when this device is used with an open drain TXD output on the microprocessor CAN controller. An adequate external pull up resistor must be used to make sure the TXD output of the microprocessor maintains adequate bit timing input to the CAN transceiver.

8.3.7.9 CAN Bus Short Circuit Current Limiting

The TCAN1043xx-Q1 has several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting (dominant and recessive). The device has TXD dominant time out which prevents permanently having the higher short circuit current of dominant state in case of a system fault. During CAN communication the bus switches between dominant and recessive states, thus the short circuit current can be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in the termination resistors and common mode choke ratings, the average short circuit current is typically used. The percentage dominant is limited by the TXD dominant time out and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and interframe space. These make sure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current can be calculated with Equation 1.

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times I_{OS(SS)\_REC}) + (\%DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%Receive \times I_{OS(SS)\_REC}] \quad (1)$$

Where:

- $I_{OS(AVG)}$ is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current

Note

The short circuit current and possible fault cases of the network can be taken into consideration when sizing the power ratings of the termination resistance and other network components.

8.4 Device Functional Modes

The device has four main operating modes: Normal mode, Standby mode, Silent mode and Sleep mode, and one transitional mode called Go-to-Sleep mode. Operating mode selection is made via the nSTB and EN input terminals in conjunction with supply conditions and wake events.

Table 8-3. Operating Modes

V_{CC} and V_{IO}	V_{SUP}	EN	nSTB	WAKERQ Flag	Mode	Driver	Receiver	RXD	Bus Bias	INH
> UV_{VCC} and > UV_{VIO}	> UV_{VSUP}	H	H	X	Normal	Enabled	Enabled	Mirrors Bus State	V_{CC}/2	ON
> UV_{VCC} and > UV_{VIO}	> UV_{VSUP}	L	H	X	Silent	Disabled (OFF)	Enabled	Mirrors Bus State	V_{CC}/2	ON
> UV_{VCC} and> UV_{VIO}	> UV_{VSUP}	H	L	Cleared	Go-to-Sleep(1)	Disabled (OFF)	Low Power Bus Monitor Enabled (ON)	High or High Z (no V_{IO})	Weak pull to GND	ON(2)
				Cleared	Sleep(3)	Disabled (OFF)	Low Power Bus Monitor Enabled (ON)	High or High Z (no V_{IO})	Weak pull to GND	OFF
				Set	Standby	Disabled (OFF)	Low Power Bus Monitor Enabled (ON)	LOW signals wake up	Weak pull to GND	ON
> UV_{VCC} and > UV_{VIO}	> UV_{VSUP}	L	L	X	Standby	Disabled (OFF)	Low Power Bus Monitor Enabled (ON)	LOW signals wake up	Weak pull to GND	ON
< UV_{VCC} and V_{VIO}	> UV_{VSUP}	X	X	X	Sleep	Disabled (OFF)	Low Power Bus Monitor Enabled (ON)	High or High Z (no V_{IO})	Weak pull to GND	OFF (High Z)
X	< UV_{VSUP}	X	X	X	Protected	Disabled (OFF)	Disabled (OFF)	High Z	High Z	OFF (High Z)

(1) Go-to-sleep: Transitional mode for EN = H, nSTB = L until $t_{go\_to\_sleep}$ timer has expired
(2) The INH pin transitions to high Z (off) after $t_{go\_to\_sleep}$ timer has expired
(3) Mode change from Go-to-Sleep mode to sleep mode once $t_{go\_to\_sleep}$ timer has expired

8.4.1 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 8-2 and Figure 8-3.

In the recessive bus state the bus is biased to a common mode of approximately V_{CC}/2 (2.5 V) via the high resistance internal input resistors of the receiver of each node on the bus. Recessive is equivalent to a logic high and is typically a differential voltage on the bus of approximately 0 V.

The dominant bus state is when the bus is driven differentially by one or more drivers. Current flows through the termination resistors and generates a differential voltage on the bus. Dominant is equivalent to a logic low and is a differential voltage on the bus greater than the minimum threshold for a CAN dominant. A dominant state overwrites the recessive state.

During arbitration, multiple CAN nodes may transmit a dominant bit at the same time. In this case, the differential voltage of the bus is greater than the differential voltage of a single driver.

The host microprocessor of the CAN node uses the TXD terminal to drive the bus and receives data from the bus on the RXD terminal.

The TCAN1043xx-Q1 transceivers has a third bus state in low power standby mode where the bus terminals are weakly biased to ground via the high resistance internal resistors of the receiver. See Figure 8-2 and Figure 8-3.

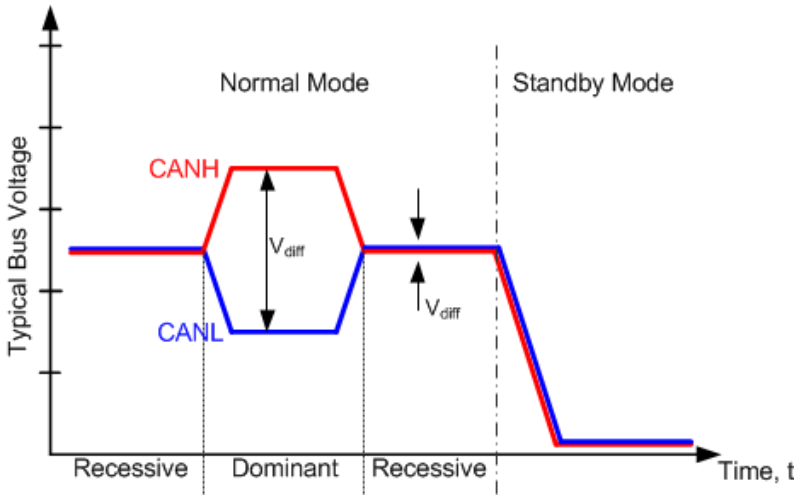
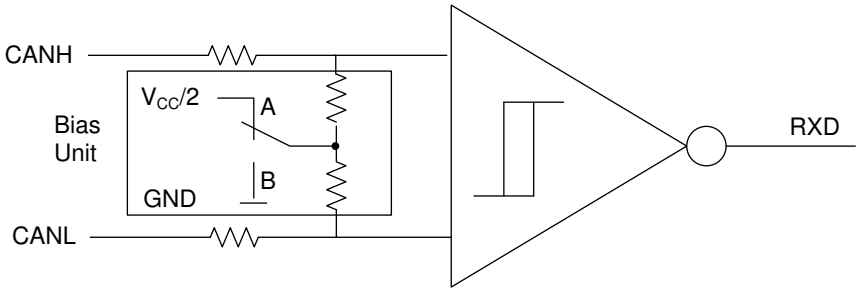
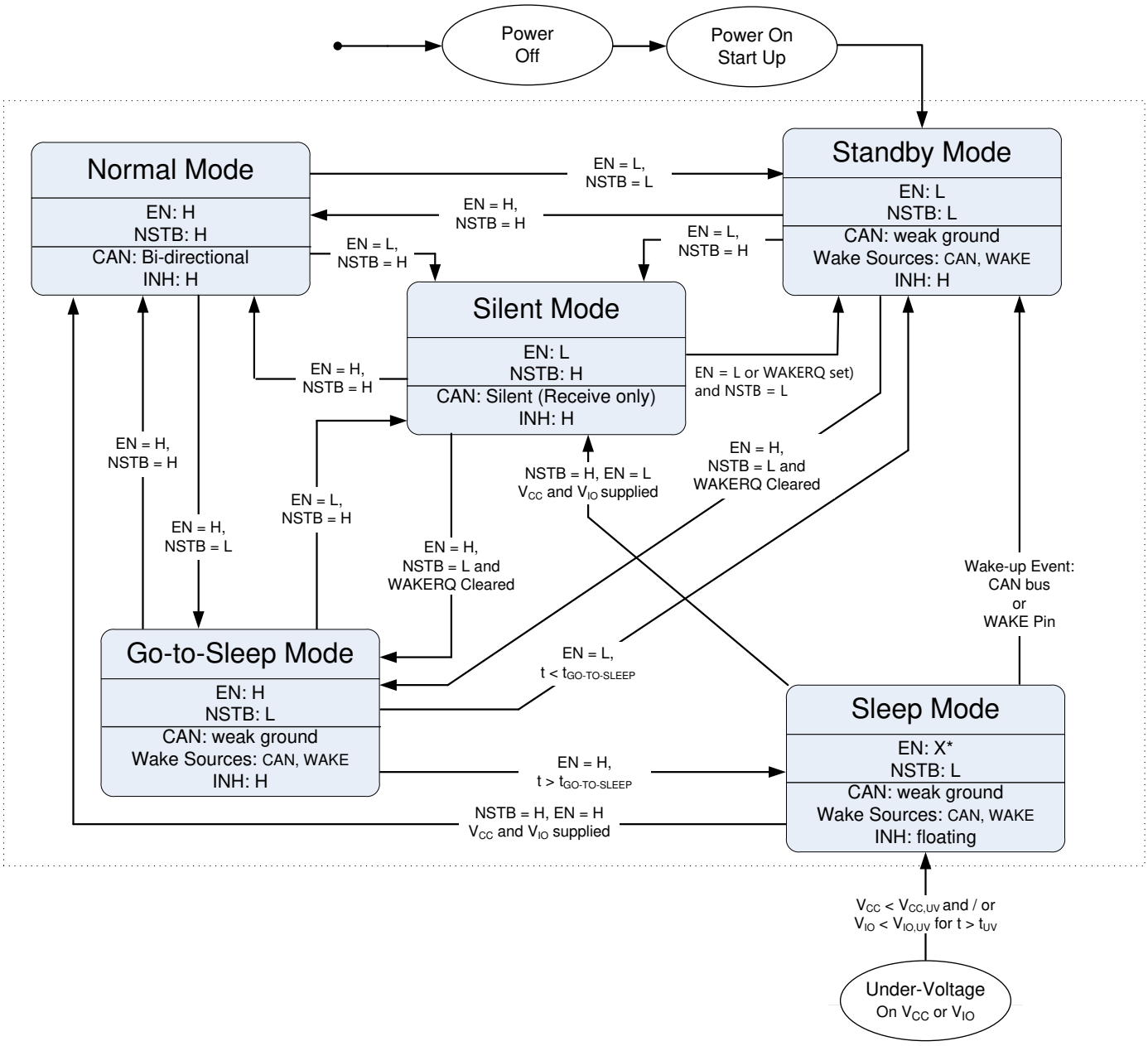


Figure 8-2. Bus States (Physical Bit Representation)



A. Normal and Silent Modes
B. Sleep and Standby Modes

Figure 8-3. Bias Unit (Recessive Common Mode Bias) and Receiver



*The enable pin can be in a logical high or low state while in sleep mode but since it has an internal pull-down, the lowest possible power consumption occurs when the pin is left either floating or pulled low externally.

Figure 8-4. State Diagram

8.4.2 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD

Entering Normal mode clears both the WAKERQ and PWRON flags.

8.4.3 Silent Mode

Silent mode is commonly referred to as listen only and receive only mode. In this mode, the CAN driver is disabled but the receiver is fully operational and CAN communication is unidirectional into the device. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD terminal.

In Silent mode, the PWRON, and Local Failure Flags can be polled.

8.4.4 Standby Mode

Standby mode is a low power mode where the driver and receiver are disabled, reducing current consumption. However, this is not the lowest power mode of the device since the INH terminal is on, allowing the rest of the system to resume normal operation.

During standby mode, a wake up request (WAKERQ) is indicated by the RXD terminal being low. The wake up source is identified via the nFAULT pin after the device is returned to normal mode.

8.4.5 Go-to-Sleep Mode

Go-to-Sleep mode is the transitional mode of the device from any state to sleep. In this state the driver and receiver are disabled, reducing the current consumption. However, the INH terminal is on allowing the rest of the system to resume normal operation. If the device is held in this state for time ≥ $t_{go\_to\_sleep}$ the device transitions to sleep mode and the INH is turned off (high Z).

Entering Go-to-Sleep Mode from standby mode is gated if the WAKERQ flag is set. Once this flag is cleared the transition is no longer gated.

8.4.6 Sleep Mode with Remote Wake and Local Wake Up Requests

Sleep mode is the lowest power mode of the device. The CAN driver and main receiver are turned off and bi-directional CAN communication is not possible.

The low power receiver with bus monitor and WAKE circuits are supplied via the V_{SUP} supply terminal. The low power receiver is able to monitor the bus for any activity that validates the wake up pattern (WUP) requirements, and the WAKE monitoring circuit monitors for state changes on the WAKE terminal for a local wake up (LWU) event. The V_{CC} and V_{IO} supplies can be turned off or be controlled via the INH output for additional system level current savings.

The valid wake up sources in sleep mode are:

- Remote wake request: CAN bus activity that validates the WUP requirements
- Local wake up (LWU) request: state change on WAKE terminal

Additionally, EN and nSTB can be used to change modes if both V_{CC} and V_{IO} are powered.

If a bus wake up pattern (WUP) or local wake up (LWU) event occurs, the internal WAKERQ flag is set and the device transitions to standby mode which in turn sets the INH output high. The wake up source recognition flag (WAKESR) is set either high or low to identify which wake event occurred. This flag can be polled via the nFAULT pin after the device is returned to normal mode and only until there have been four recessive to dominant transitions on the TXD pin.

The wake source (WAKESR) flag has two states:

- Low: This indicates that the wake up source was via the WAKE pin.
- High: This indicates that a remote wake request via the CAN bus occurred.

If both a local wake and a remote wake request occur, the device indicates whichever event was completed first.

The device transitions into sleep mode if at any time either or both the V_{CC} or V_{IO} supplies have an under voltage condition that lasts longer than timer t_{UV}. If V_{IO} remains active in sleep mode, the recommendation is to drive the EN pin low once the device has transitioned into sleep mode to reduce the current consumption due to the internal pull-down on the EN terminal.

8.4.6.1 Remote Wake Request via Wake Up Pattern (WUP)

The TCAN1043xx-Q1 use the multiple filtered dominant wake up pattern (WUP) from ISO 11898-2 (2016) to qualify bus activity. The WUP is active for both sleep and standby modes and results in the RXD terminal being driven low after a valid pattern is received.

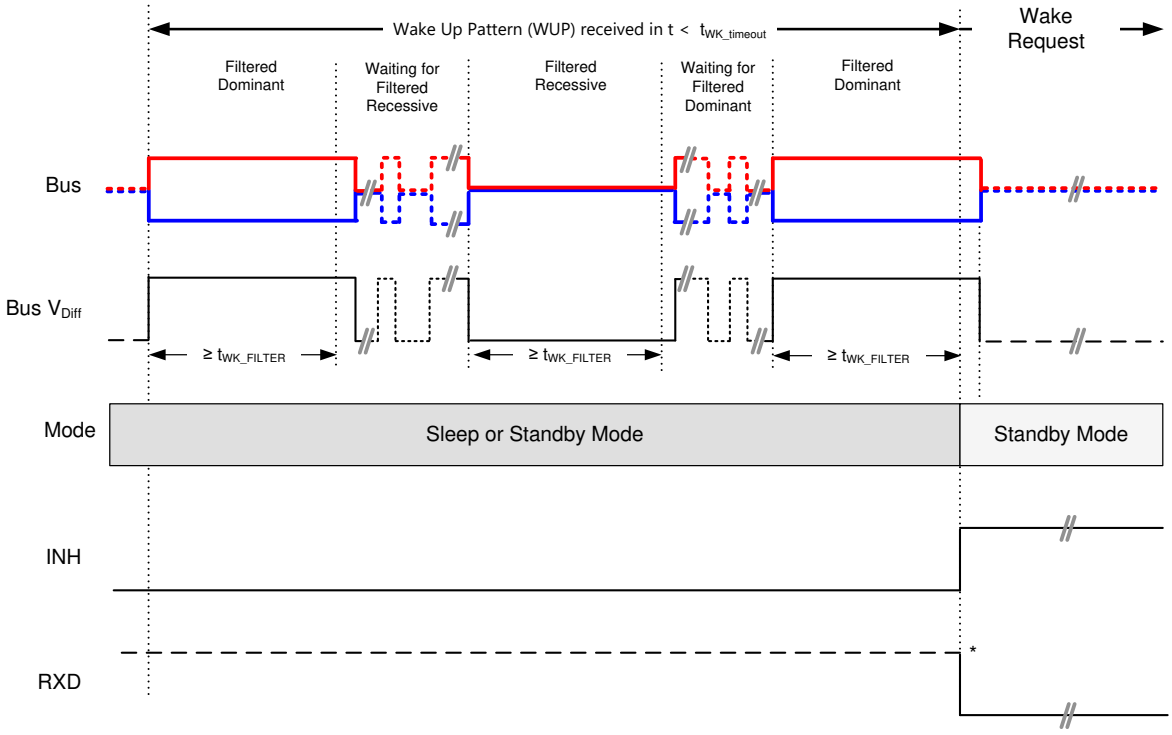
The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and transition to standby mode, drives the INH output high and sets the RXD terminal low (if V_{IO} is present) to signal the wake up request.

For a dominant or recessive to be considered “filtered”, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP and thus no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a wake request may be generated. Bus state times greater than $t_{WK\_FILTER(MAX)}$ will always be detected as part of a WUP and thus a wake request will always be generated. See Figure 8-5 for the timing diagram of the WUP.

The pattern and t_{WK_FILTER} time used for the WUP and wake request prevents noise and bus stuck dominant faults from causing false wake requests while allowing any CAN or CAN FD message to initiate a wake request.

If the device is switched to normal mode or an under voltage event occurs on either the V_{CC} or V_{IO} supplies, the wake request is lost.

ISO 11898-2 (2016) has two sets of times for a short and long wake up filter times. The t_{WK_FILTER} timing for the TCAN1043xx-Q1 devices have been picked to be within the min and max values of both filter ranges. This timing has been chosen such that a single bit time at 500 kbps, or two back to back bit times at 1 Mbps triggers the filter in either bus state.



The RXD pin is only driven once V_{IO} is present.

Figure 8-5. Wake Up Pattern (WUP)

For an additional layer of robustness and to prevent false wake-ups, these devices implement a timeout feature. For a remote wake up event to successfully occur, the entire WUP must be received within the timeout value t < $t_{WK\_timeout}$ (see Figure 8-5). If not, the internal logic is reset and the part remains in its current state without waking up. The full pattern must then be retransmitted, conforming to the constraints mentioned in this section and shown in figure Figure 8-5.

8.4.6.2 Local Wake Up (LWU) via WAKE Input Terminal

The WAKE terminal is a high voltage input terminal which can be used for local wake up (LWU) requests via a voltage transition. The terminal triggers a local wake up (LWU) event on either a low-to-high, or a high-to-low transition since it has a bi-directional input threshold (falling or rising edge).

This terminal may be used with a switch to V_{SUP} or to ground. If the terminal is unused it should be pulled to ground or V_{SUP} to avoid unwanted parasitic wake up events.

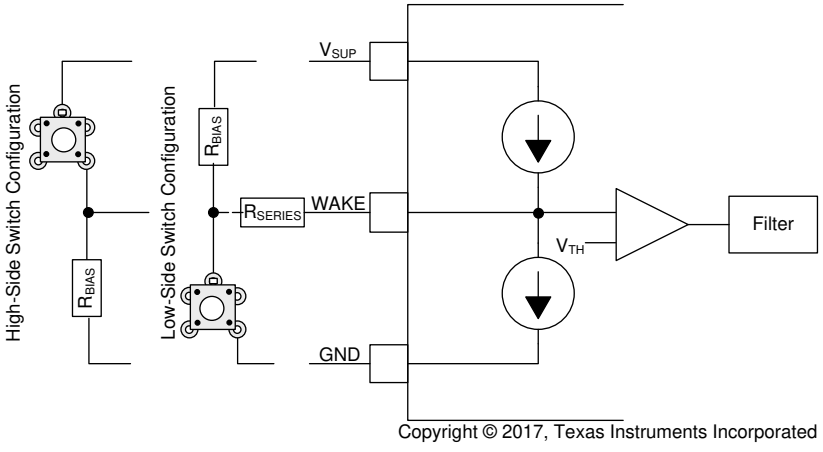


Figure 8-6. TCAN1043xx-Q1 WAKE Circuit Example

Figure 8-6 shows two possible configurations for the WAKE terminal, the low-side and high side switch configurations. The objective of the series resistor, R_{SERIES}, is to protect the WAKE pin of the transceiver from over current conditions that may occur in the event of a ground shift or ground loss. The minimum value of R_{SERIES} can be calculated using the maximum supply voltage, V_{SUPMAX} and the maximum allowable current of the WAKE pin, $I_{IO(WAKE)}$. R_{SERIES} is calculated using:

$$R_{SERIES} = V_{SUPMAX} / I_{IO(WAKE)} \quad (2)$$

If the battery voltage never exceeds 58 V DC, then the R_{SERIES} value is approximately 20 kΩ.

The R_{BIAS} resistor is used to set the static voltage level of the WAKE pin when the switch is not in use. When the switch is in use in a high-side switch configuration, the R_{BIAS} resistor in combination with the R_{SERIES} resistor sets the WAKE pin voltage appropriately above the V_{IH} threshold. The maximum value of R_{BIAS} can be calculated using the maximum supply voltage, V_{SUPMAX}, the maximum WAKE threshold voltage V_{IH}, the maximum WAKE input current I_{IH} and the series resistor value R_{SERIES}. R_{BIAS} is calculated using:

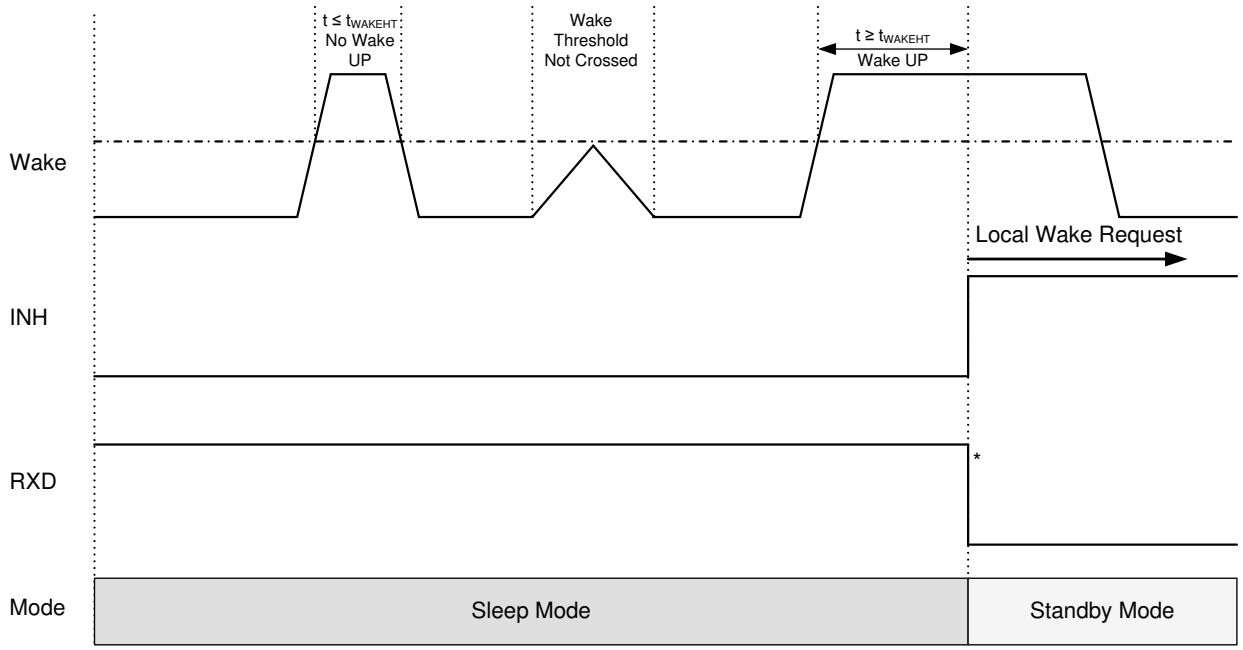
$$R_{BIAS} < ((V_{SUP} - V_{IH}) / I_{IH}) - R_{SERIES} \quad (3)$$

If the battery voltage never exceed 58 V DC, then the R_{BIAS} resistor value must be less than 60 kΩ.

For lower current consumption, the low-side switch configuration is the ideal architecture.

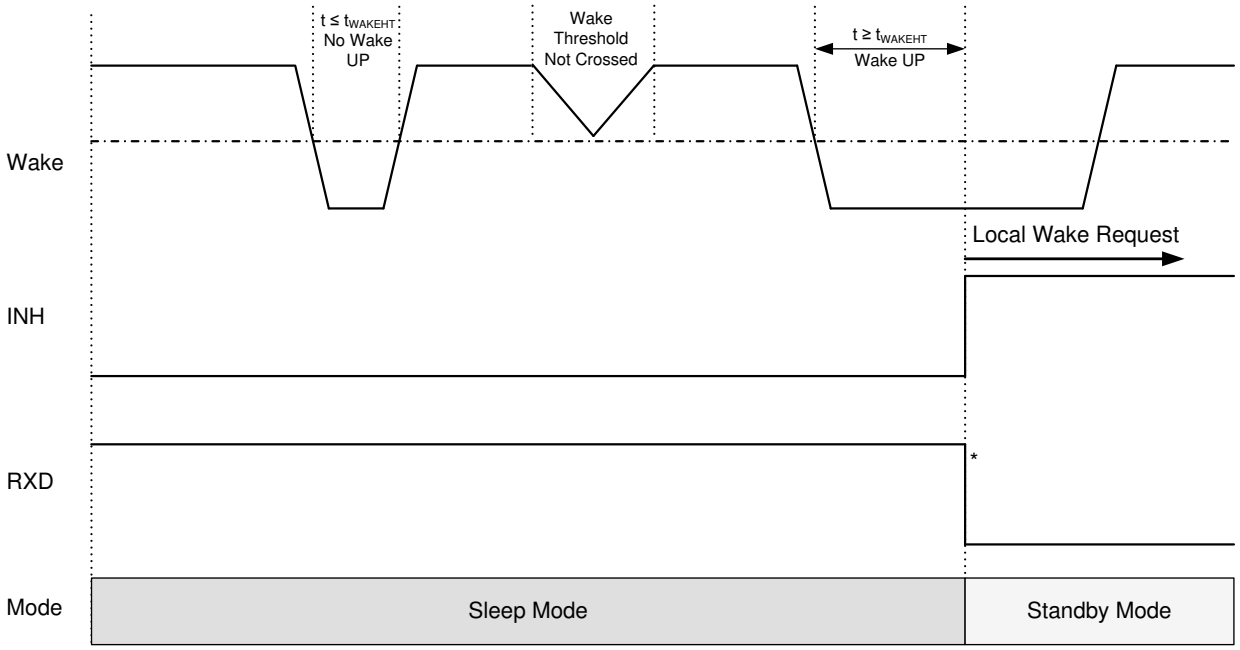
The LWU circuitry is active in *Section 8.4.6*, *Section 8.4.4* and *Section 8.4.5*. If a valid LWU event occurs the device transitions to standby mode. The LWU circuitry is not active in Normal mode or Silent mode.

To minimize system level current consumption, the internal bias voltages of the terminal follows the state on the terminal with a delay of $t_{WAKE(min)}$. A constant high level on WAKE has an internal pull-up to V_{SUP} and a constant low level on WAKE has an internal pull-down to GND. This minimizes the current flowing into the WAKE pin under these steady-state conditions so that it does not need to be factored into calculations of the total draw from V_{SUP}.



The RXD pin is only driven once V_{IO} is present.

Figure 8-7. Local Wake Up – Rising Edge



The RXD pin is only driven once V_{IO} is present.

Figure 8-8. Local Wake Up – Falling Edge

8.4.7 Driver and Receiver Function Tables

Table 8-4. Driver Function Table

DEVICE MODE	TXD INPUTS(1)	BUS OUTPUTS(2)		DRIVEN BUS STATE(3)
		CANH	CANL	
Normal	L	H	L	Dominant
	H or Open	Z	Z	Common Mode Biased to V_{CC}/2
Silent	X	Z	Z	Common Mode Biased to V_{CC}/2
Standby	X	Z	Z	Common Mode Biased to GND
Go-to-Sleep	X	Z	Z	Common Mode Biased to GND
Sleep	X	Z	Z	Common Mode Biased to GND

(1) H = high level, L = low level, X = irrelevant.
(2) H = high level, L = low level, Z = high Z receiver bias.
(3) For Bus state and bias see Figure 3 and Figure 4.

Table 8-5. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} – V_{CANL}$	BUS STATE	RXD TERMINAL(1)
Normal	V_{ID} ≥ 0.9 V	Dominant	L
	0.5 V < V_{ID} < 0.9 V	Indeterminate	Indeterminate
	V_{ID} ≤ 0.5 V	Recessive	H
	Open (V_{ID} ≈ 0 V)	Open	H
Standby	V_{ID} ≥ 1.15 V	Dominant	H L if either remote or local wake events have occurred
	V_{ID} ≤ 0.4 V	Indeterminate	
	0.5 V < V_{ID} < 1.15 V	Recessive	
	Open (V_{ID} ≈ 0 V)	Open	
Sleep and Go-to-Sleep (WUP Monitor)	V_{ID} ≥ 1.15 V	Dominant	H L if either remote or local wake events have occurred and V_{IO} is present. Tri-State if V_{IO} or V_{SUP} are not present
	0.4 V , V_{IO} < 1.15 V	Indeterminate	
	V_{ID} ≤ 0.4 V	Recessive	
	Open (V_{ID} ≈ 0 V)	Open	

(1) H = high level, L = low level

8.4.8 Digital Inputs and Outputs

All devices have a V_{IO} supply that is used to set the digital input thresholds and digital output levels. The input thresholds are ratio metric to the V_{IO} supply using CMOS input levels, making them scalable for µPs with digital IOs from 2.8 V to 5 V. The high level output voltages for the RXD and nFAULT output pins are driven to V_{IO} level for logic high output.

8.4.9 INH (Inhibit) Output

The inhibit output terminal is used to control system power management devices allowing for extremely low system current consumption in sleep mode. This terminal can be used to enable and disable local power supplies. The pin has two states: driven high and high impedance (High Z).

When high (on), the terminal shows V_{SUP} minus a diode voltage drop. In the high impedance state, the output is left floating. The INH pin is high for normal, silent, Go-to-Sleep, and standby modes. INH is low when in sleep mode.

Note

This terminal is considered a “high voltage logic” terminal, not a power output. Thus, can be used to drive the EN terminal of the system power management device and not used as a switch for the power management supply. This terminal is not reverse battery protected and can not be connected outside the system module.

9 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TCAN1043xx-Q1 transceivers are typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. These types of applications usually also include power management technology that allows for power to be gated to the application via an enable (EN) or inhibit (INH) pin. A single 5-V regulator can be used to drive both V_{CC} and V_{IO} as shown in Figure 9-1, or independent 5-V and 3.3-V regulators can be used to drive V_{CC} and V_{IO} separately as shown in Figure 9-2. The bus termination is shown for illustrative purposes.

9.2 Typical Application

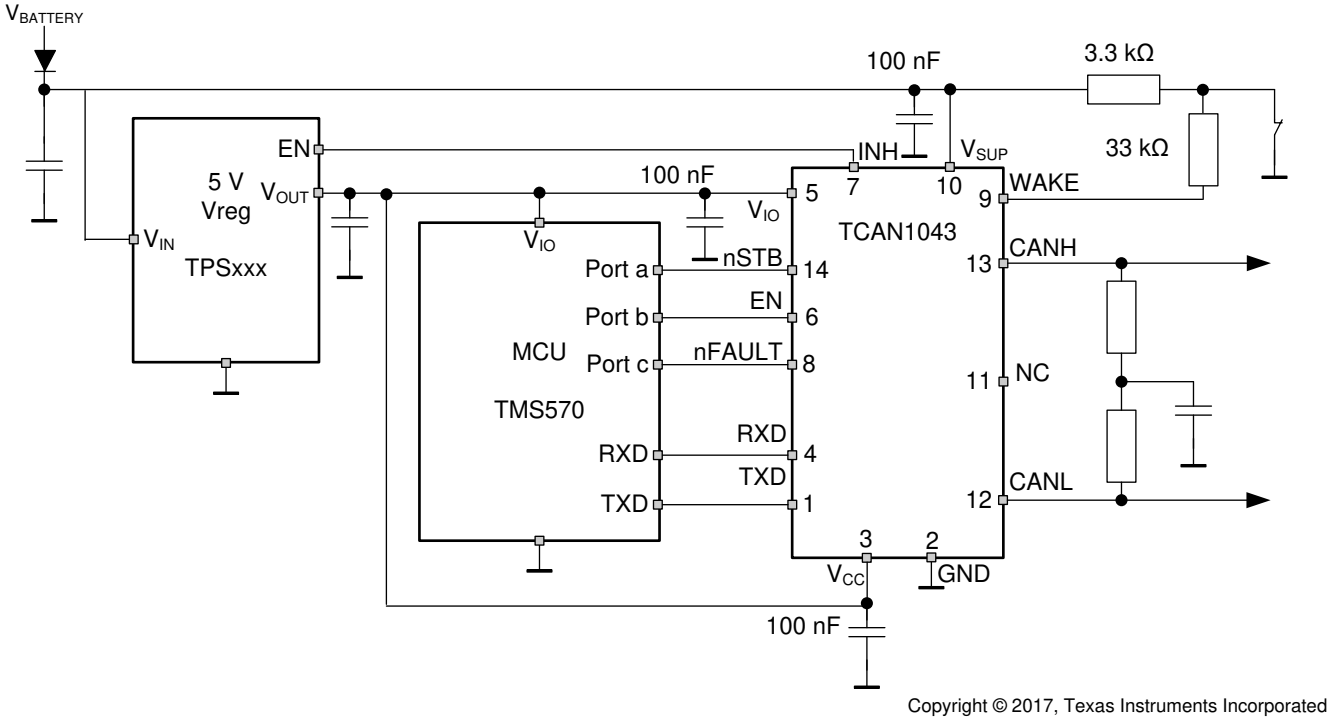


Figure 9-1. Typical CAN Bus Application Using TCAN1043xx-Q1 With 5 V µC

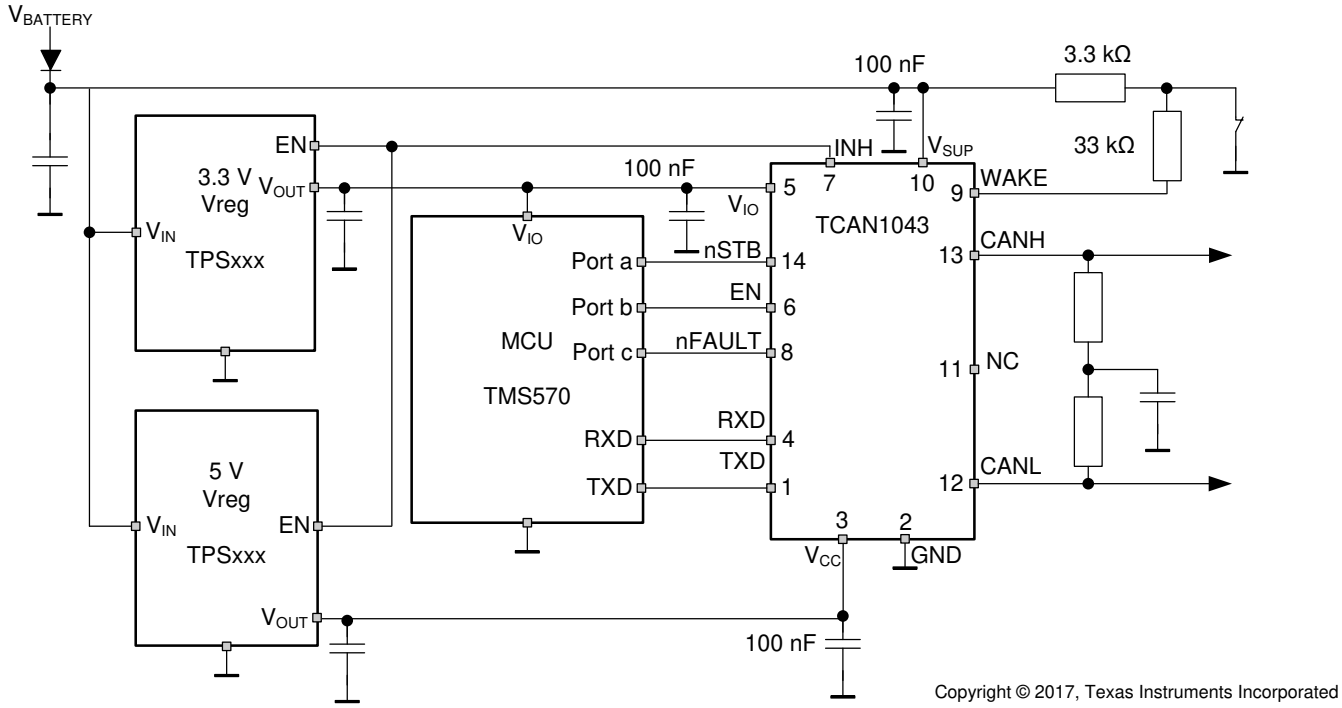


Figure 9-2. Typical CAN Bus Application Using TCAN1043xx-Q1 With 3.3 V µC

9.2.1 Design Requirements

9.2.1.1 Bus Loading, Length and Number of Nodes

A typical CAN application can have a maximum bus length of 40 meters and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1043xx-Q1 family.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In ISO 11898-2 the driver differential output is specified with a bus load that can range fro 50 Ω to 65 Ω where the differential output must be greater than 1.5 V. The TCAN1043xx-Q1 family is specified to meet the 1.5-V requirement down to 50 Ω and is specified to meet 1.4-V differential output at 45Ω bus load. The differential input resistance of the TCAN1043xx-Q1 is a minimum of 30 kΩ. If 100 TCAN1043xx-Q1 transceivers are in parallel on a bus, this is equivalent to a 300-Ω differential load in parallel with the nominal 60 Ω bus termination which gives a total bus load of 50 Ω. Therefore, the TCAN1043xx-Q1 family theoretically supports over 100 transceivers on a single bus segment. However for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is much lower. Bus length can also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design to for robust network operation.

9.2.2 Detailed Design Procedures

9.2.2.1 CAN Termination

The ISO11898-2 standard specifies the interconnect to be a single twisted pair cable (shielded or unshielded) with 120 Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line can be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus must be kept as short as possible to minimize signal reflections. The termination can be in a node but is generally not recommended, especially if the node can be removed from the bus. Termination must be carefully placed so that it is not removed from the bus. System level CAN implementations such as CANopen allow for different termination and cabling concepts for example to add cable length.

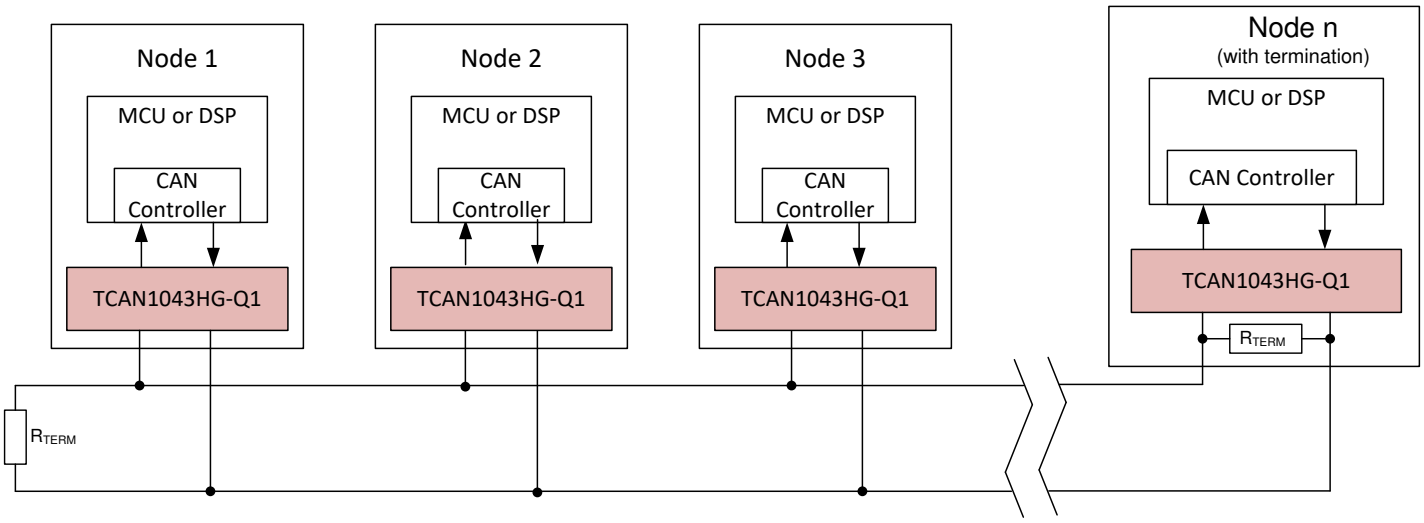


Figure 9-3. Typical CAN Bus Application

Termination can be a single 120-Ω resistor at the ends of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired then “split termination” can be used, see Figure 9-4. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltage levels at the start and end of message transmissions.

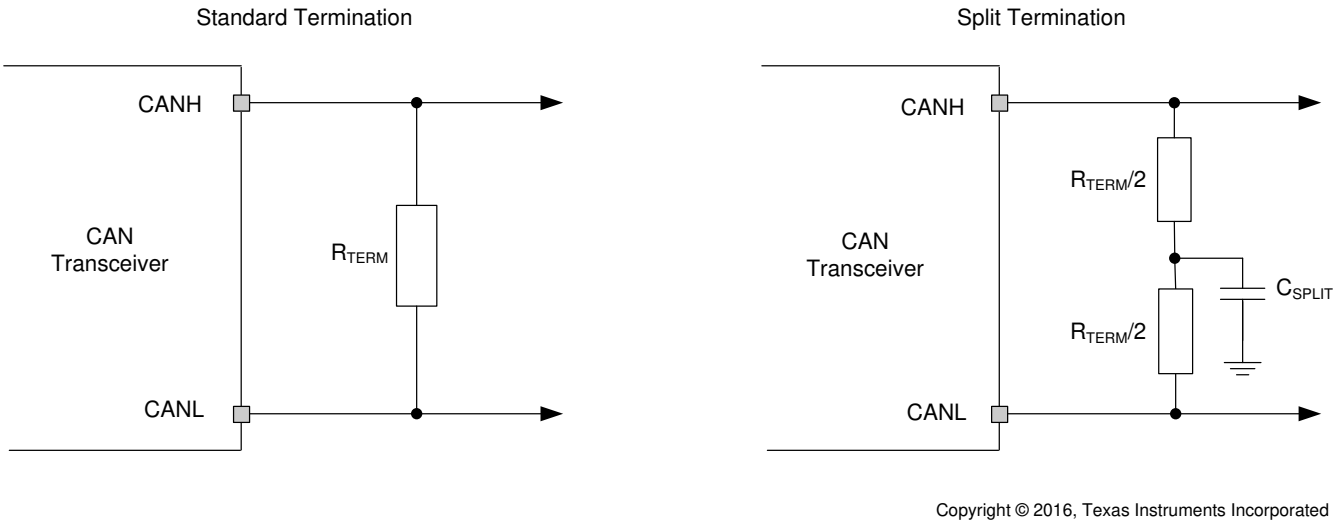


Figure 9-4. CAN Bus Termination Concepts

9.2.3 Application Curves

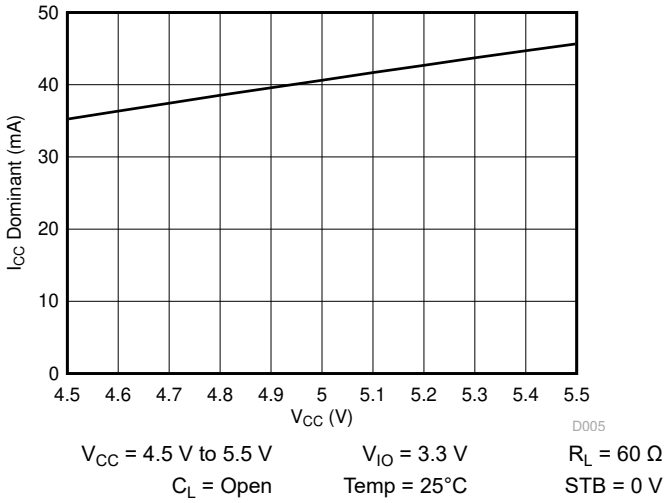


Figure 9-5. I_{CC} Dominant Current over V_{CC} Supply Voltage

9.3 Power Supply Recommendations

The TCAN1043xx-Q1 device is designed to operate with a main V_{CC} input voltage supply range between 4.5 V and 5.5 V. The device also has an IO level shifting supply input, V_{IO} , designed for a range between 2.8 V and 5.5 V. For reliable operation at all data rates and supply voltages, each supply can be decoupled with a 100 nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

9.4 Layout

9.4.1 Layout

Robust and reliable bus node design often requires the use of external transient protection devices to protect against transients that can occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques can be applied during PCB design.

9.4.1.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector to prevent transients, ESD, and noise from propagating onto the board. In this layout example a transient voltage suppression (TVS) device, D1, has been shown as added protection. The production solution can be either bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C6 and C8, typical values range from 10 pF to 100 pF, depending on how many nodes are on the CAN bus. Additionally (not shown) a series common mode choke (CMC) can be placed on the CANH and CANL lines between the TCAN1043xx-Q1 transceiver and the connector.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Use supply (V_{CC}) and ground planes to provide low inductance as high-frequency current will follow the path of least impedance and not the path of least resistance.
- Use at least two vias for supply (V_{CC}, V_{IO}, V_{SUP}) and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.
- Bypass and bulk capacitors must be placed as close as possible to the supply terminals of transceiver, examples are C4 on the V_{CC} supply net, C5 on the V_{IO} supply net and C9 on the V_{SUP} supply net, all of which are typically chosen as 100 nF.

- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R6 and R7 (both 60 ohms), with the center or split tap of the termination connected to ground via capacitor C7 (typically 4.7 nF, but can go up to 100 nF). Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to make sure the terminating node is not removed from the bus thus also removing the termination. See the application section for information on power ratings needed for the termination resistor(s).
- To limit current of digital lines, series resistors can be used as in R2, R3 and R5, but are not required.
- Terminal 1: R1 is shown optionally for the TXD input of the device. If an open drain host processor is used, this is mandatory to make sure the bit timing into the device is met. R1 is typically 10 kΩ.
- Terminal 9: SW1 is oriented in a low-side configuration which is used to implement a local WAKE event. The series resistor R10 is needed for protection against over current conditions to limit the current into the WAKE pin when the ECU has lost the ground connection. The pull-up resistor R9 is required to provide sufficient current during stimulation of a WAKE event. See the application section for more information on calculating both the R9 and R10 values.
- Terminal 14: Is shown assuming the mode terminal, nSTB, is used. If the device is only be used in normal mode, R5 is not needed and R4 can be used for the pull-up resistor to V_{IO}, R5 is typically 10 kΩ.

9.4.2 Layout Example

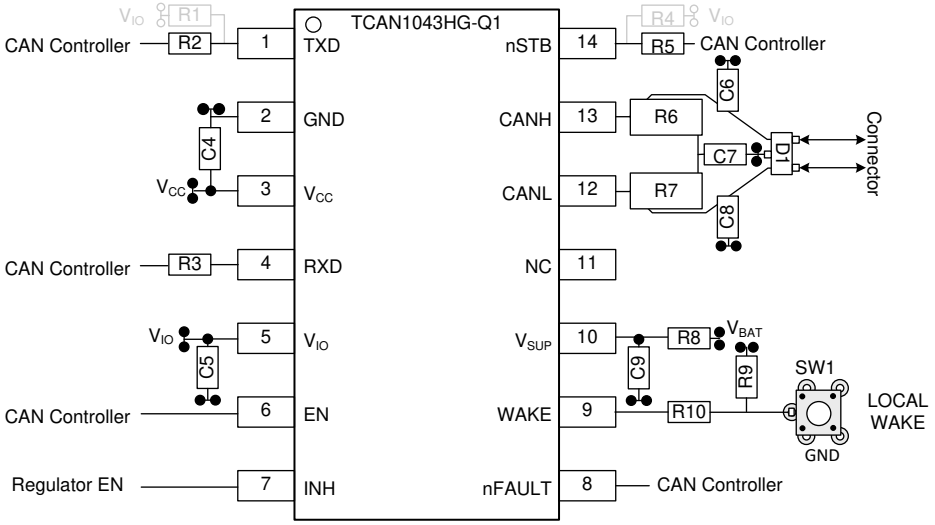


Figure 9-6. TCAN1043xx-Q1 Layout Example

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

Changes from Revision E (January 2021) to Revision F (November 2023)	Page
• Changed the *Device Information* table to the *Packaging Information* table	1
• Deleted the *Description (continued)* section	1
• Changed the last sentence of the *CAN Bus Failure Fault Flag* section	20

Changes from Revision D (July 2019) to Revision E (January 2021)	Page
• Added Functional Safety to the *Features* list	1

Changes from Revision C (October 2018) to Revision D (July 2019)	Page
• Changed the second sentence in the *CAN Bus Dominant Fault* section	22

Changes from Revision B (May 2018) to Revision C (October 2018)	Page
• Updated I_{CC} dominant with bus fault	7
• Added footnote for I_{IH} and I_{IL}	7
• Changed the Under-Voltage callout in Figure 8-4	24
• Added sentence: "This minimizes the current flowing into the WAKE pin..." to the last paragraph in *Local Wake Up (LWU) via WAKE Input Terminal*	29

Changes from Revision A (December 2017) to Revision B (May 2018)	Page
• Updated note 1 to: AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-01 specification	5
• Added Note 2 To ESD Specification Table	6
• Updated IEC 61000-4-2 Unpowered Contact Dicharge to ±15kV	6
• Changed Max t_{WK_FILTER} to 1.8µs	10

Changes from Revision * (November 2017) to Revision A (December 2017)	Page
• Changed status from *Advance Information* to *Production Data*	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN1043DMTRQ1	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1043	Samples
TCAN1043DMTTQ1	ACTIVE	VSON	DMT	14	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1043	Samples
TCAN1043DQ1	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1043	Samples
TCAN1043DRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1043	Samples
TCAN1043GDMTRQ1	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1043	Samples
TCAN1043GDMTTQ1	ACTIVE	VSON	DMT	14	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1043	Samples
TCAN1043GDQ1	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1043	Samples
TCAN1043GDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1043	Samples
TCAN1043HDMTRQ1	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1043	Samples
TCAN1043HDMTTQ1	ACTIVE	VSON	DMT	14	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1043	Samples
TCAN1043HDQ1	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1043	Samples
TCAN1043HDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1043	Samples
TCAN1043HGDMTRQ1	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1043	Samples
TCAN1043HGDMTTQ1	ACTIVE	VSON	DMT	14	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 125	1043	Samples
TCAN1043HGDQ1	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1043	Samples
TCAN1043HGDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1043	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

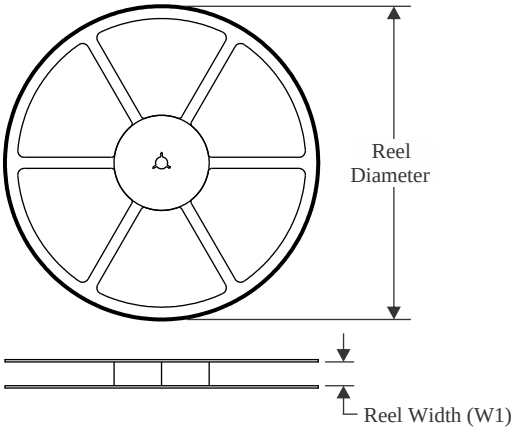
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

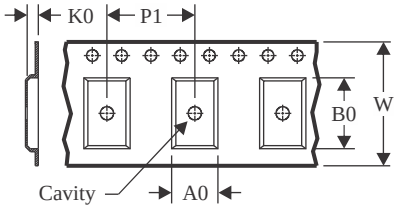
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

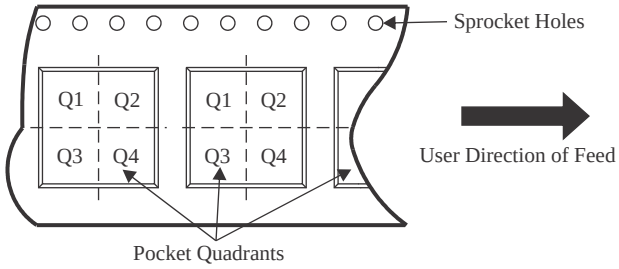


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

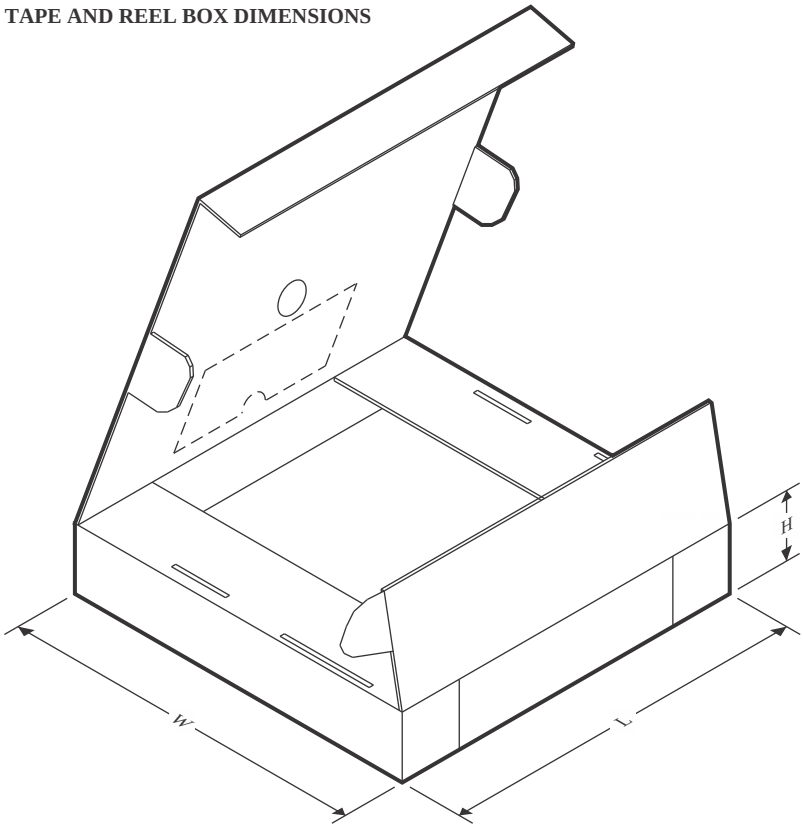
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1043DMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1043DMTTQ1	VSON	DMT	14	250	180.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1043DRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TCAN1043GDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1043GDMTTQ1	VSON	DMT	14	250	180.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1043GDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TCAN1043HDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1043HDMTTQ1	VSON	DMT	14	250	180.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1043HDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TCAN1043HGDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1043HGDMTTQ1	VSON	DMT	14	250	180.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1043HGDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TCAN1043HGDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

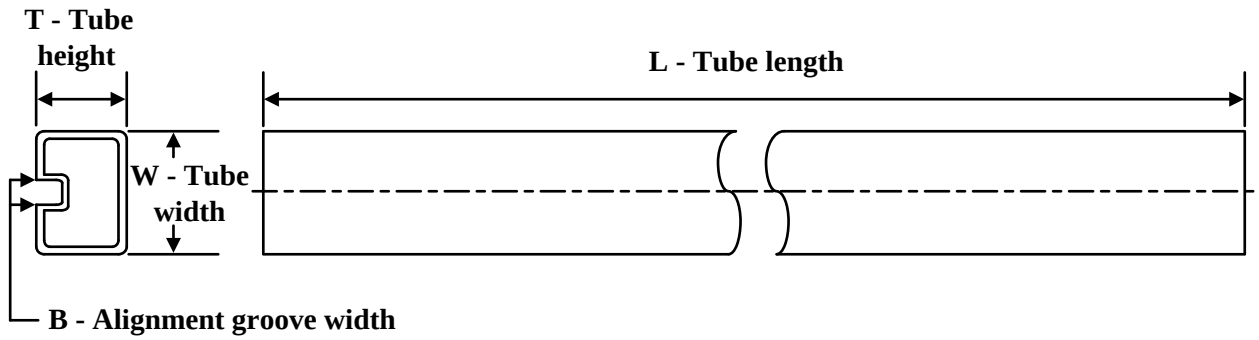
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1043DMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
TCAN1043DMTTQ1	VSON	DMT	14	250	210.0	185.0	35.0
TCAN1043DRQ1	SOIC	D	14	2500	333.2	345.9	28.6
TCAN1043GDMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
TCAN1043GDMTTQ1	VSON	DMT	14	250	210.0	185.0	35.0
TCAN1043GDRQ1	SOIC	D	14	2500	333.2	345.9	28.6
TCAN1043HDMTRQ1	VSON	DMT	14	3000	210.0	185.0	35.0
TCAN1043HDMTTQ1	VSON	DMT	14	250	210.0	185.0	35.0
TCAN1043HDRQ1	SOIC	D	14	2500	333.2	345.9	28.6
TCAN1043HGDMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
TCAN1043HGDMTTQ1	VSON	DMT	14	250	210.0	185.0	35.0
TCAN1043HGDRQ1	SOIC	D	14	2500	356.0	356.0	35.0
TCAN1043HGDRQ1	SOIC	D	14	2500	333.2	345.9	28.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TCAN1043DQ1	D	SOIC	14	50	507	8	3940	4.32
TCAN1043GDQ1	D	SOIC	14	50	507	8	3940	4.32
TCAN1043HDQ1	D	SOIC	14	50	507	8	3940	4.32
TCAN1043HGDQ1	D	SOIC	14	50	507	8	3940	4.32

GENERIC PACKAGE VIEW

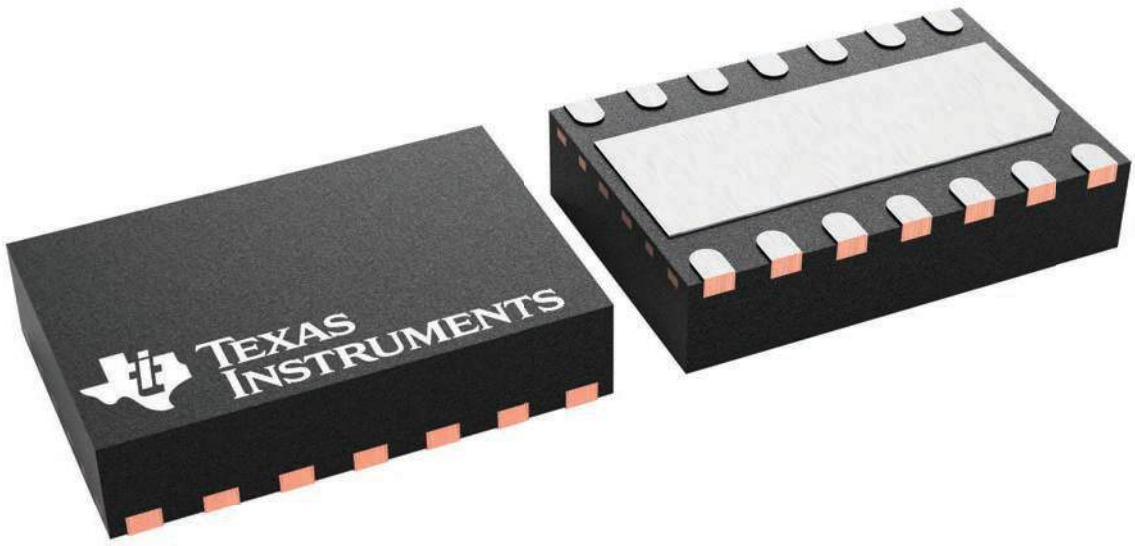
DMT 14

VSON - 0.9 mm max height

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



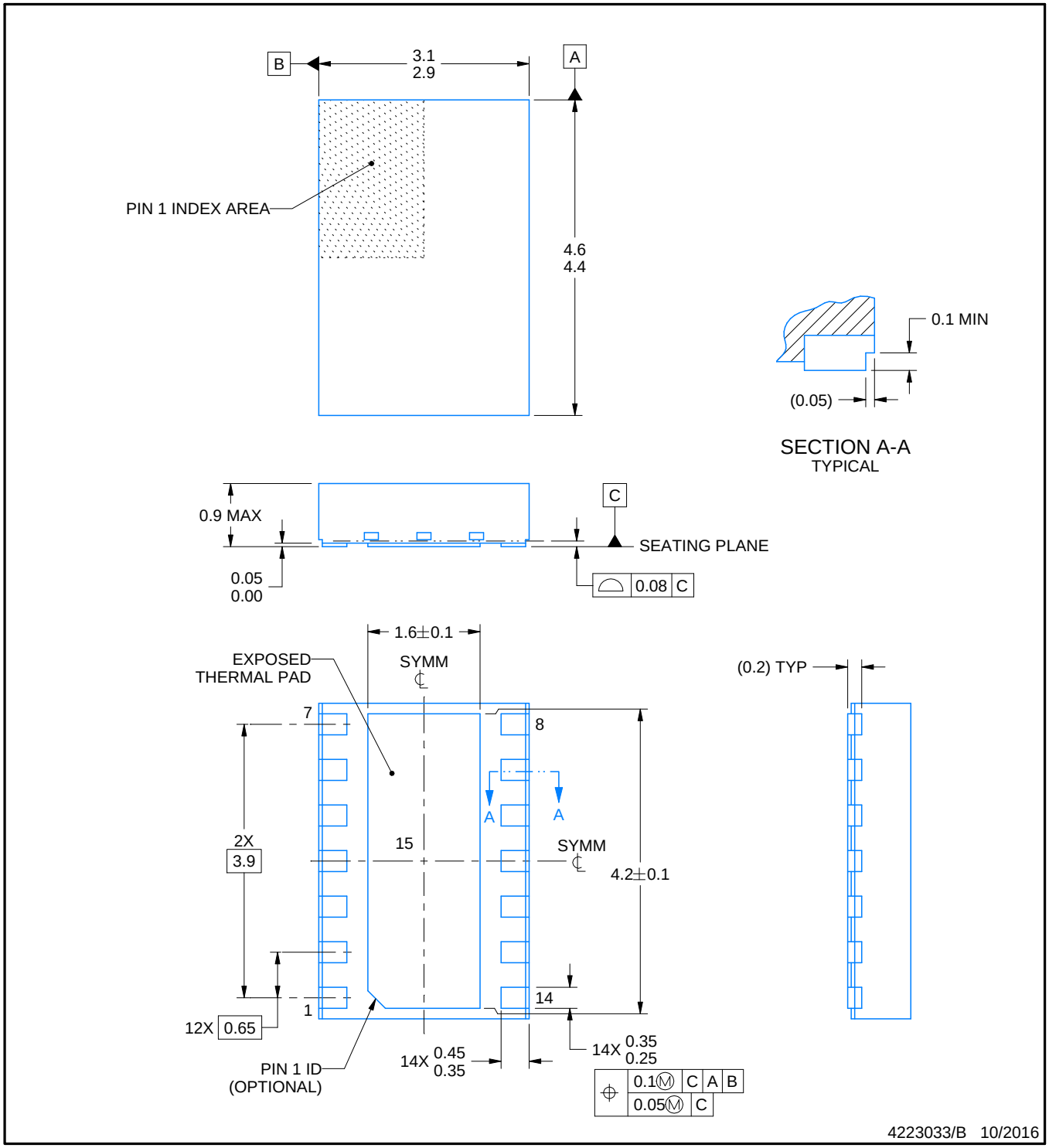
4225088/A

PACKAGE OUTLINE

DMT0014A

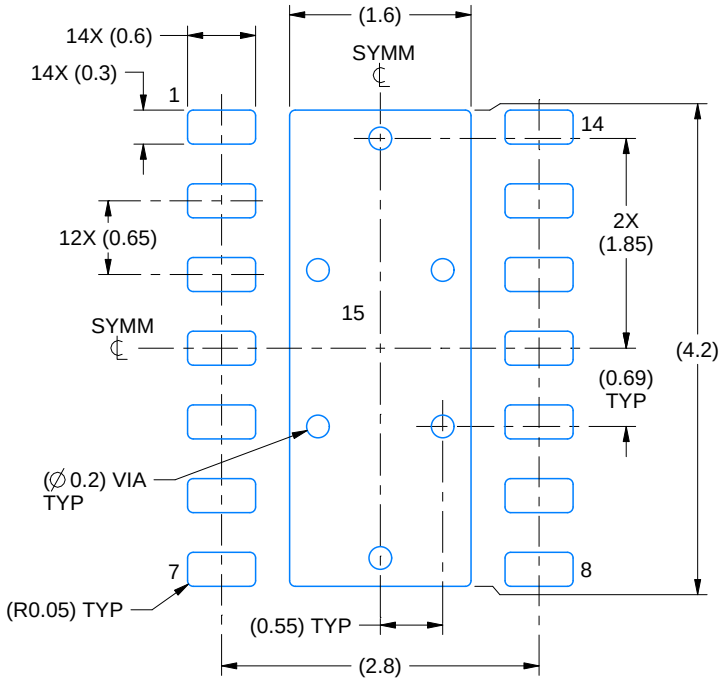
VSON - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

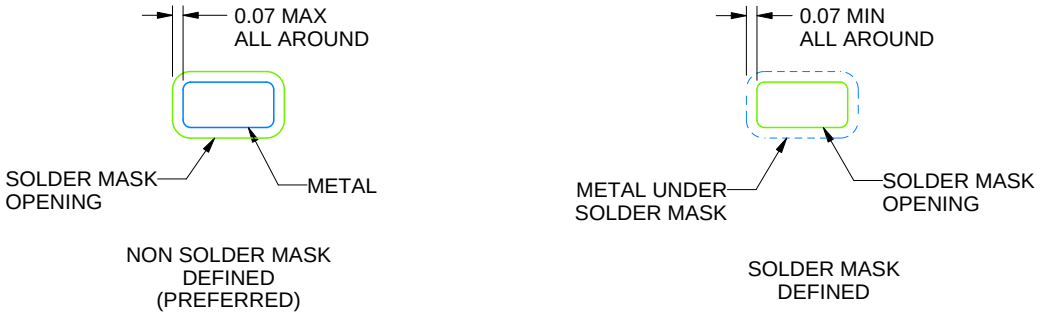


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

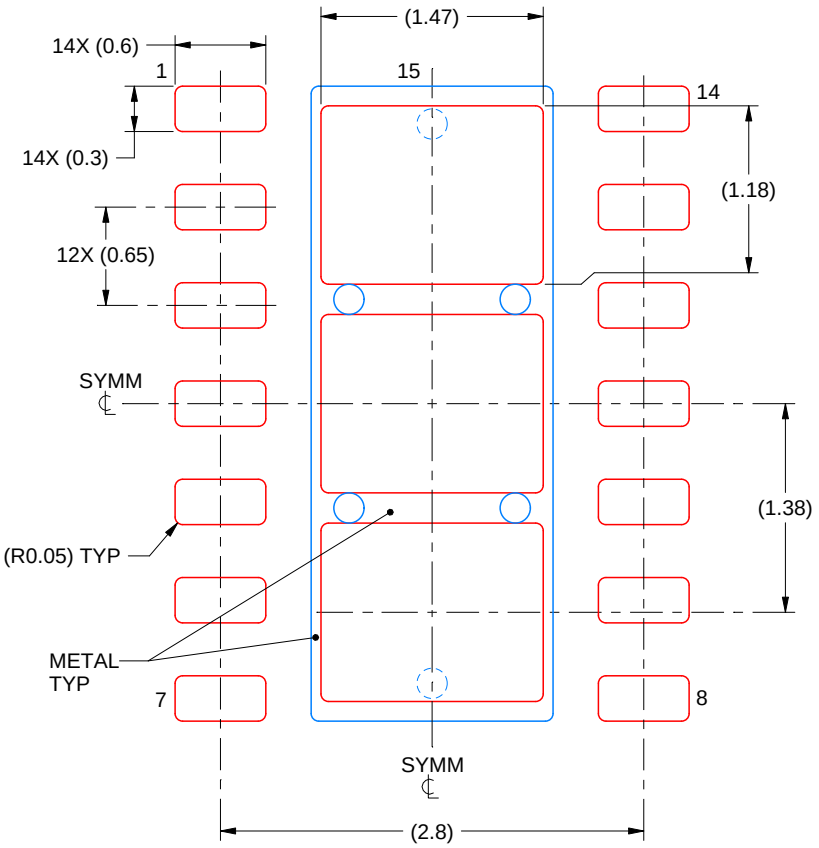


SOLDER MASK DETAILS

4223033/B 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4223033/B 10/2016

NOTES: (continued)

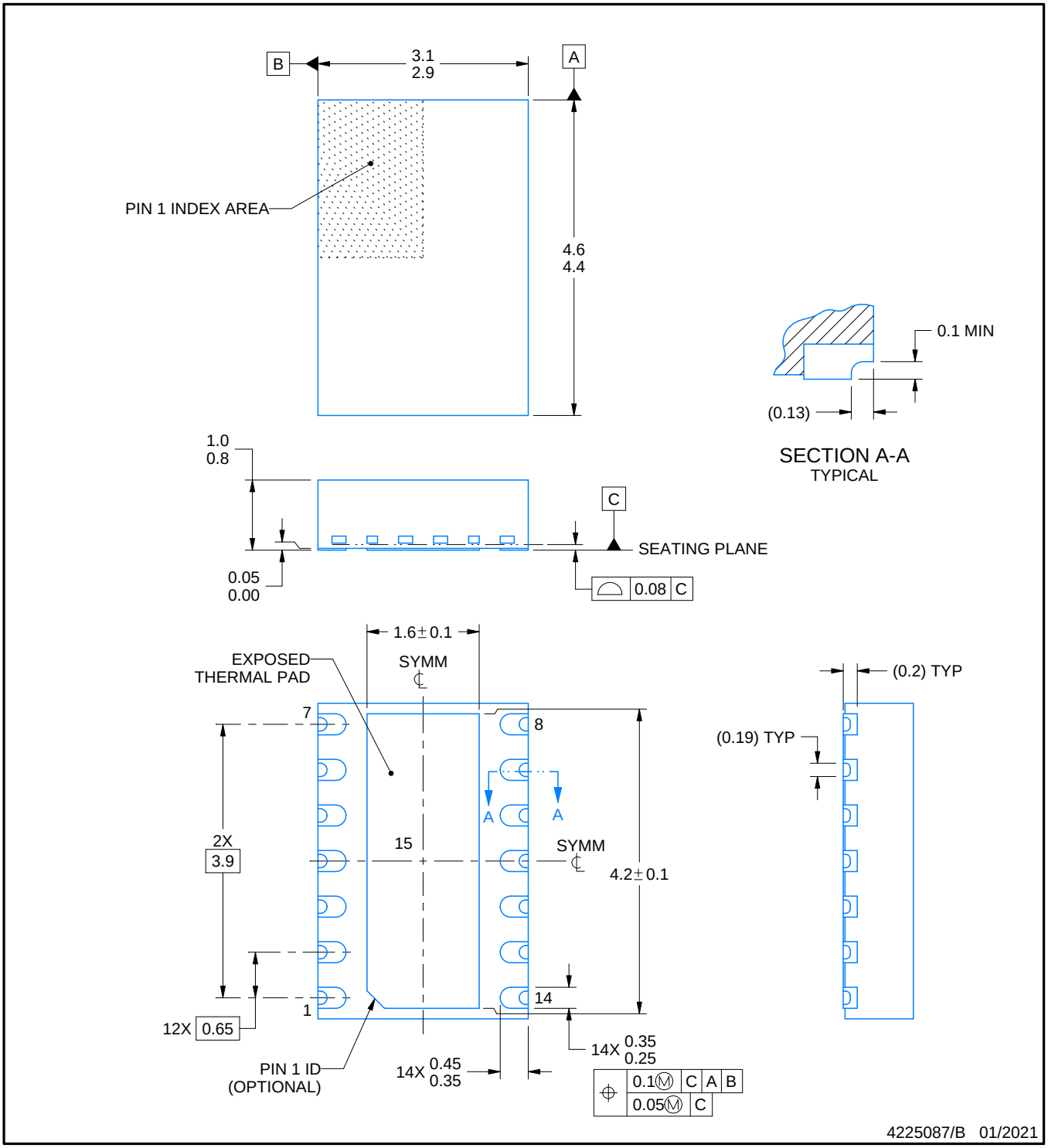
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DMT0014B

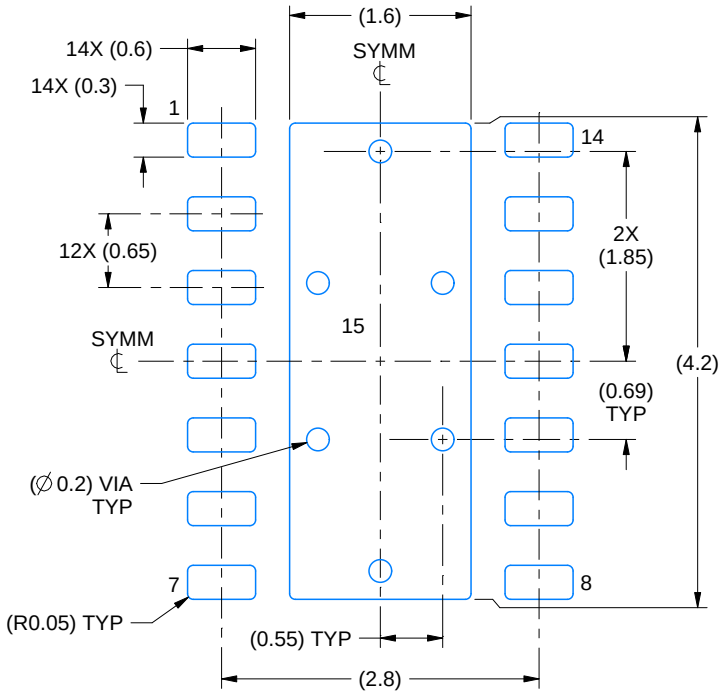
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

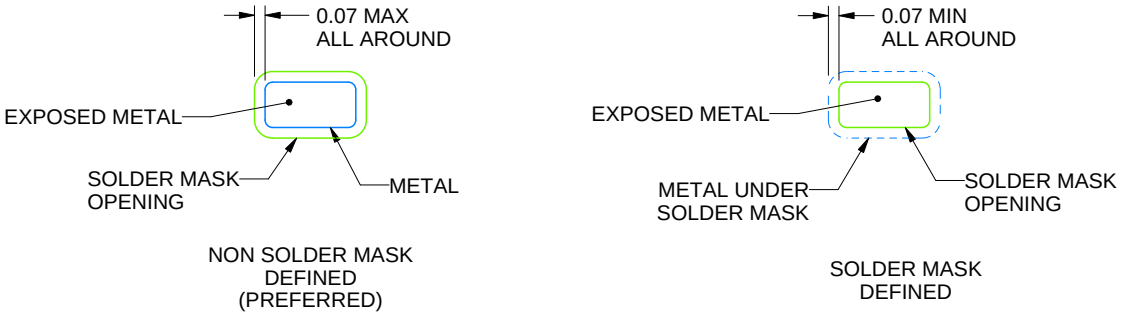


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

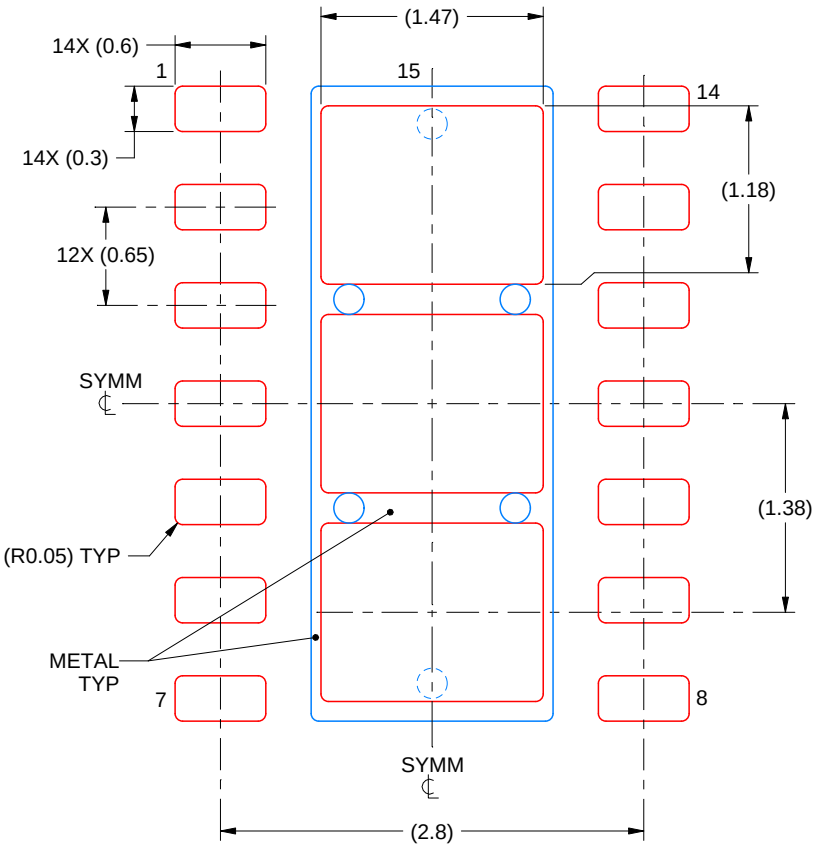


SOLDER MASK DETAILS

4225087/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

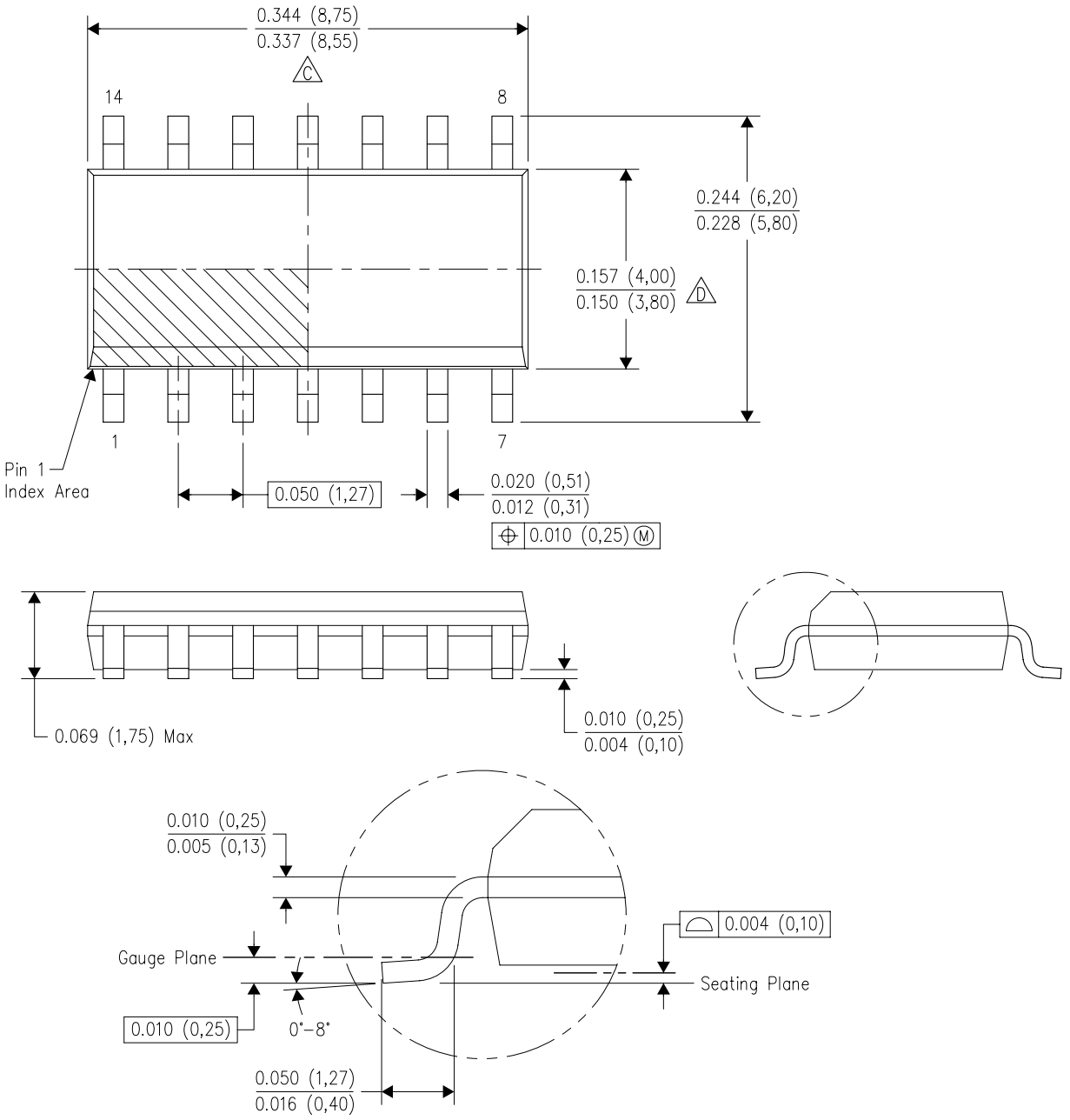
EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4225087/B 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

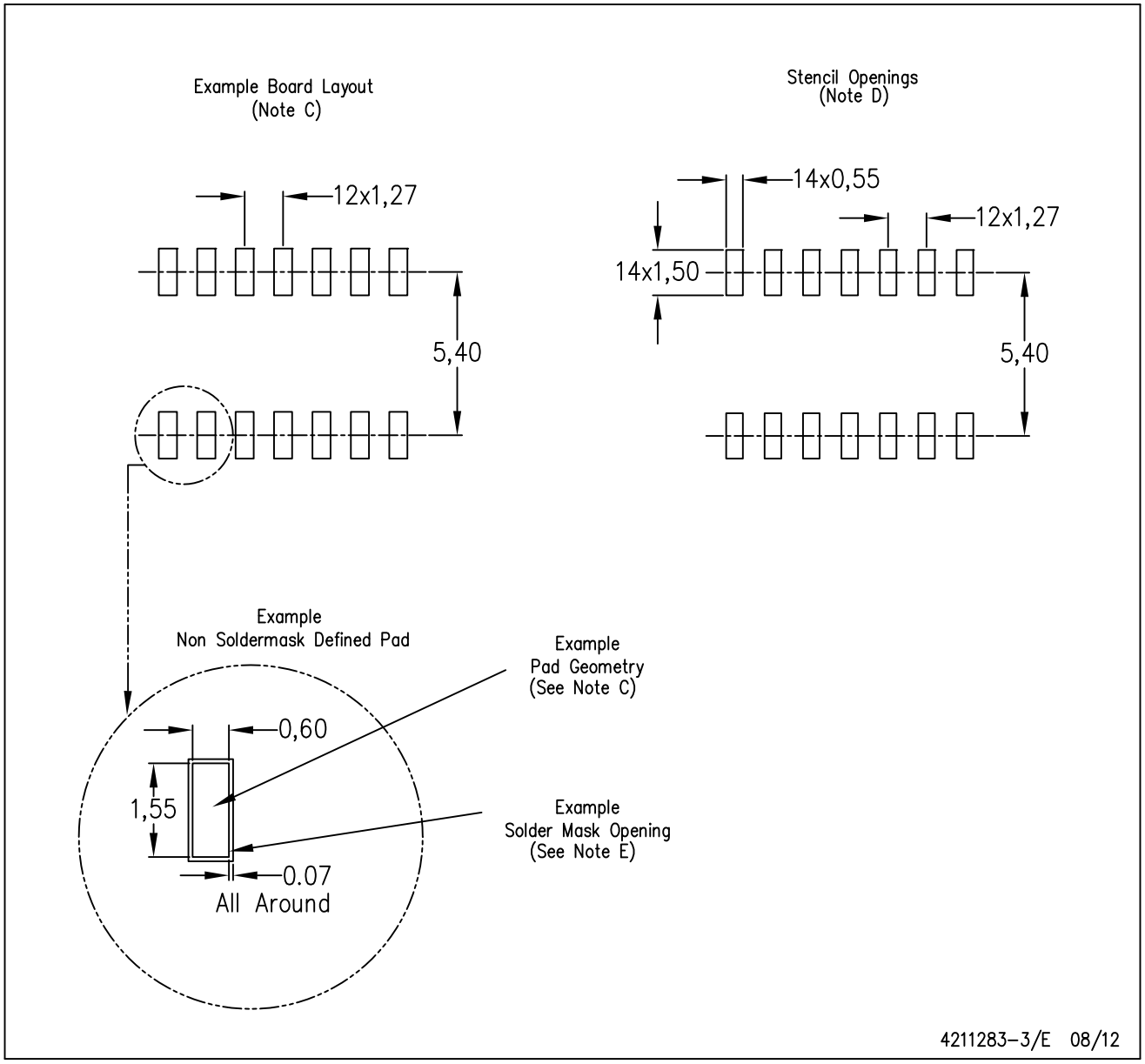
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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